VLSI AND SOFTWARE RADIOS

By John Fakatselis
Harris semi.

CONTRIBUTING ENABLING TECHNOLOGIES TO VLSI RADIOS.

- Process Technology
- Package Technology
- IC Simulation Tools
- System Simulation Tools

RADIO DESIGN EXAMPLE

- AN EXAMPLE OF A VLSI RADIO DESIGN:
  - WIRELESS LAN, BASED ON PROPOSED IEEE8021.11 SPEC.
  - RF, IF , MODEM DESIGN , AND PROTOCOL MAC.

Wireless LAN (WLAN) Markets

Current Market

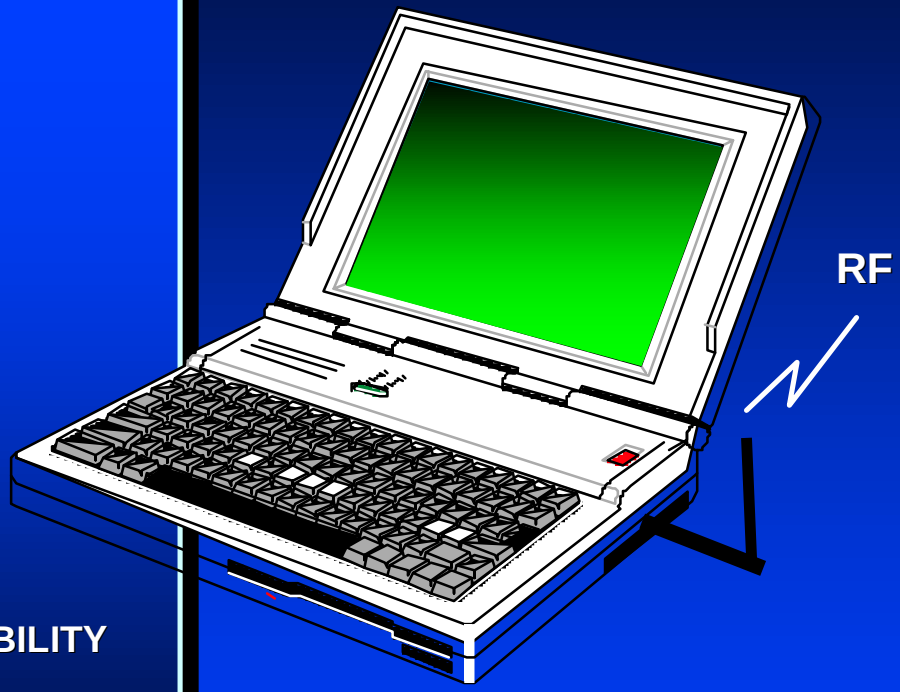
PRIMARILY AT 902 - 928MHz

- MIX OF SPREAD SPECTRUM TRANSCEIVERS WITHOUT STANDARDS
- NO COMPLIANT PROTOCOL STANDARDS
- NO INTEROPERABILITY OF EQUIPMENT
- LOW DATA RATES

Emerging Market

2.4 - 2.5GHz

- IEEE 802.11 STANDARD FOR WLANS
- COMPLIANT STANDARDS FOR INTEROPERABILITY
- CONNECTIVITY
- SUPPORT HIGHER DATA RATES
- PCMCIA LAN CARD SOLUTION
- LOWER COST
- HIGHER PERFORMANCE
  SPEED, RANGE, BATTERY LIFE

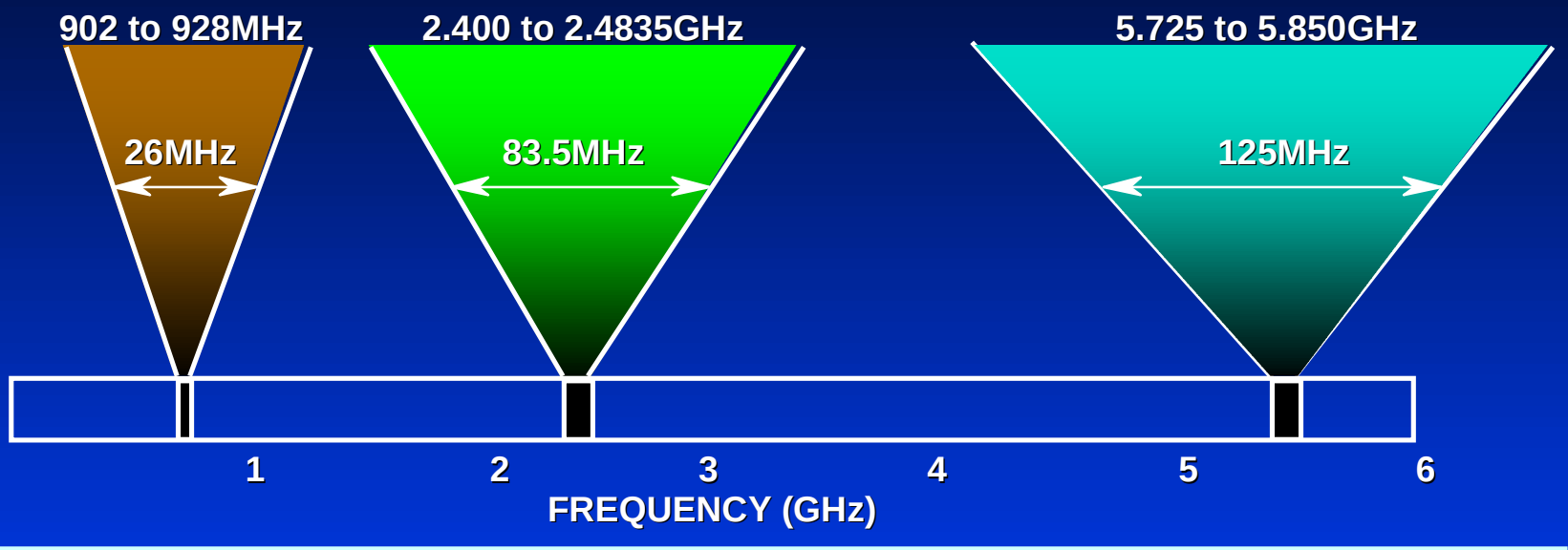


The 802.11 Wireless LAN Standard

IEEE 802.11 WLAN Standard

- IEEE WLAN WORKING GROUP WITH GLOBAL REPRESENTATION
- STANDARD FOR WLANS WITH A COMMON MULTI-USER MEDIA
- GLOBAL EQUIPMENT INTEROPERABILITY
- FREQUENCY: 2.4GHz ISM BAND (83.5MHz BW)
- MEDIUM TO HIGH DATA RATES
- APPLICATIONS RANGING FROM SMALL OFFICES TO INDUSTRIAL MANUFACTURING CAMPUSES
- SPREAD SPECTRUM TECHNOLOGY
  - Limits Transmitted Power Density
  - Provides a Robust Solution in a Multi-user Environment

Industrial, Scientific and Medical (ISM) Bands



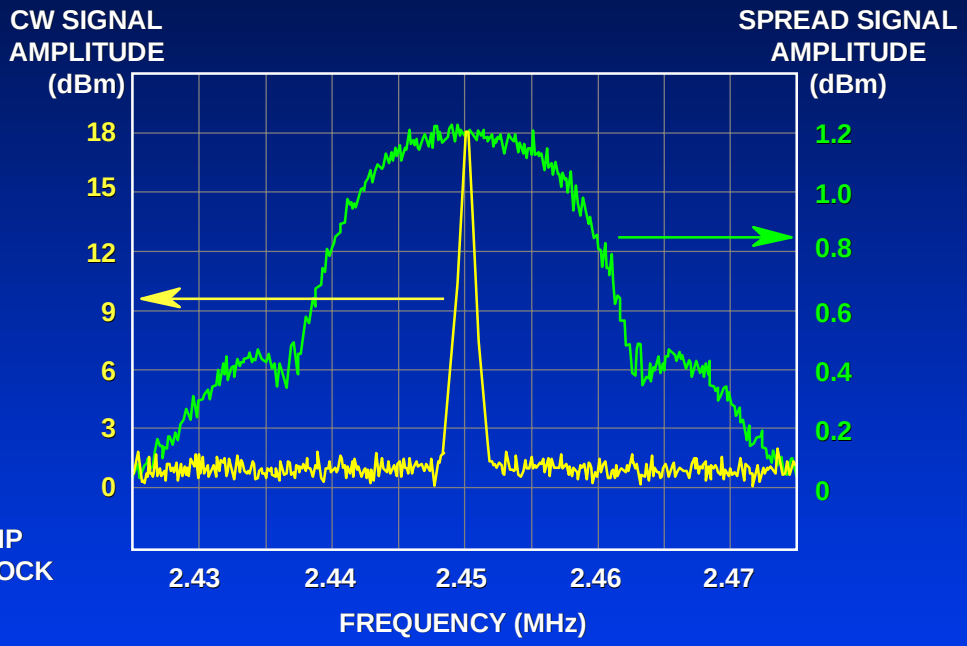
- UNLICENSED OPERATION GOVERNED BY FCC DOCUMENT 15.247, PART 15
- SPREAD SPECTRUM ALLOWED TO MINIMIZE INTERFERENCE
- 2.4GHz ISM BAND
  - More Bandwidth to Support Higher Data Rates and Number of Channels
  - Available Worldwide
  - Good Balance of Equipment Performance and Cost Compared with 5.725GHz Band
  - IEEE 802.11 Global WLAN Standard

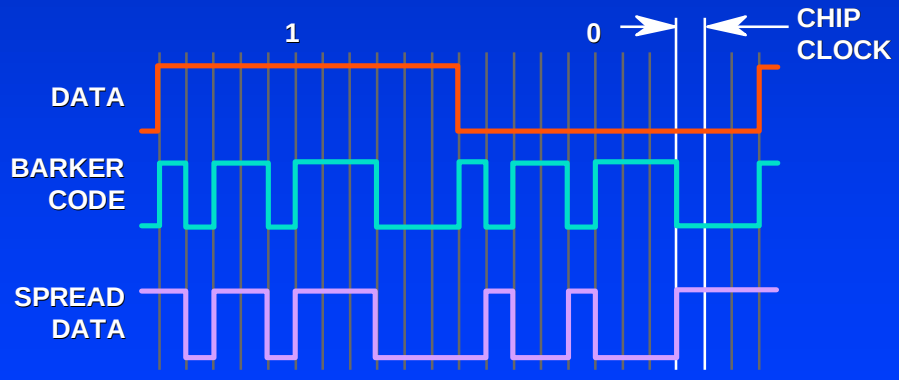
Direct Sequence Spread Spectrum

- DATA SIGNAL SPREAD BY A PN CODE
- PROPERTIES OF PN CODE
- CHIP RATE
- DS PROCESSING GAIN

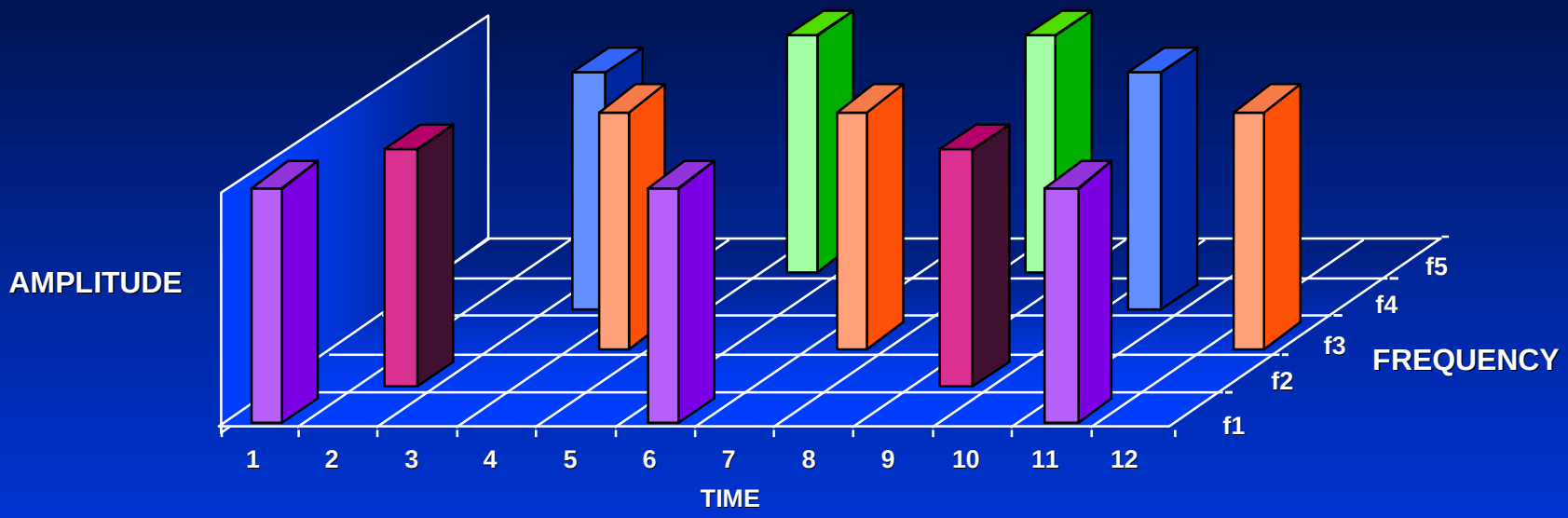
$$G_P\ (dB) = 10LOG\ \left(\frac{\text{CHIP RATE}}{\text{DATA RATE}}\right)$$

- PN CORRELATION AT RECEIVER
- PSK DATA MODULATION



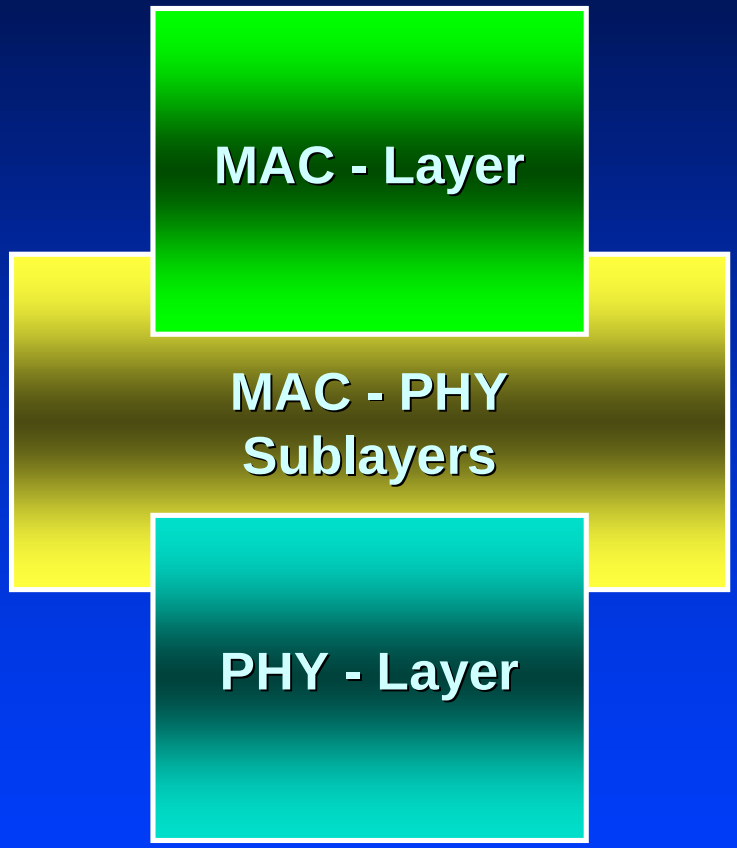


Frequency Hopping Spread Spectrum



- FSK DATA MODULATION
- PERIODIC CHANGES IN THE CARRIER FREQUENCY SPREADS THE SIGNAL
- CARRIER FREQUENCY CHANGES AT A SPECIFIED HOP RATE
- CARRIER FREQUENCY HOPS AFTER A PRESCRIBED TIME
- TOTAL SYSTEM BANDWIDTH INCLUDES ALL OF THE CHANNEL FREQUENCIES USED IN HOPPING

802.11 Protocol Layers



Media Access Control Layer

PROTOCOL AND PHYSICAL LAYER MANAGEMENT

MAC-PHY Sublayers

CONFIGURE DATA FRAMES AND PREAMBLES FOR TRANSMIT AND RECEIVE MODE

Physical Layer

RADIO TRANSMISSION MEDIA FOR EITHER DSSS, FHSS OR INFRARED

802.11 DSSS Physical Layer

MODULATION:	DPSK	
PN CODE:	11-BIT BARKER	
DATA RATE:	1Mbps/DBPSK, 2Mbps/DQPSK	
CHIPPING RATE:	11Mcps	
TRANSMIT POWER:	USA: 1W MAX.	FCC 15.247
	EUROPE: 100mW (EIRP)	ETSI 300-328
	JAPAN: 10mW / MHz	MPT ORD. 78
TRANSMIT FREQUENCY TOLERANCE:	±25ppm MAX.	
CHIP CLOCK ACCURACY:	±25ppm MAX.	
RECEIVER INPUT LEVEL SENSE:	-80dBm $8x10^{-2}$ FER (FRAME ERROR RATE)	
RECEIVER ENERGY DETECT:	20μs MAX.	
PREAMBLE LENGTH:	144 SYMBOLS	
DATA PACKET SIZE:	2048 BYTES MAX.	
ENVIRONMENT:	PACKET BURST DATA	

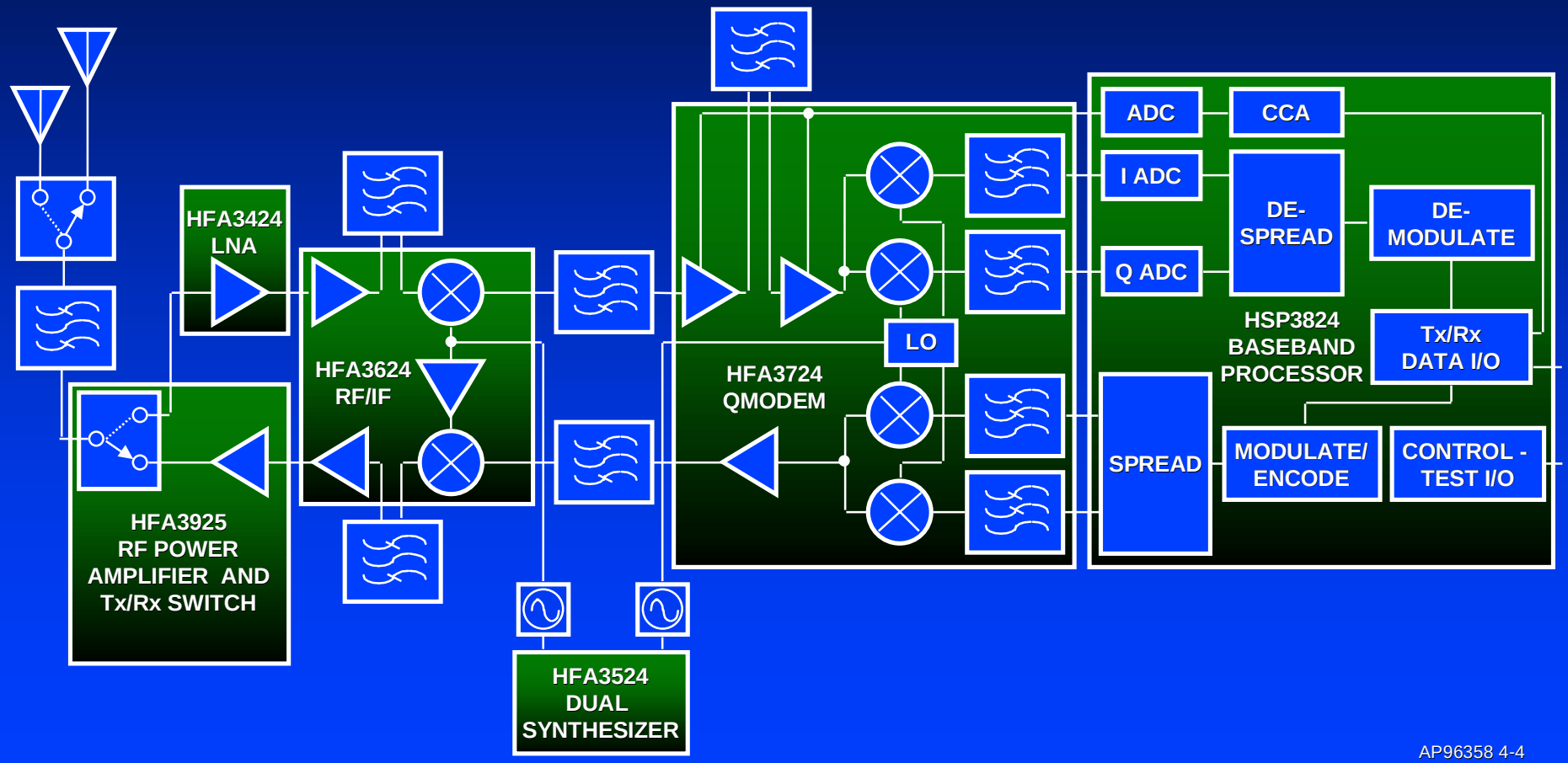

PRISM™ Chipset

WLAN Radio Requirements

- LOW COST
- HIGH DATA RATE AND HIGH THROUGHPUT
- PCMCIA COMPATIBLE
- LONG RANGE
- MOBILITY WITH ROAMING CAPABILITY
- LOW VOLTAGE, LOW POWER, BATTERY OPERATED
- HIGH LEVEL OF INTEGRATION

PRISM™ “Antenna to Bits™”

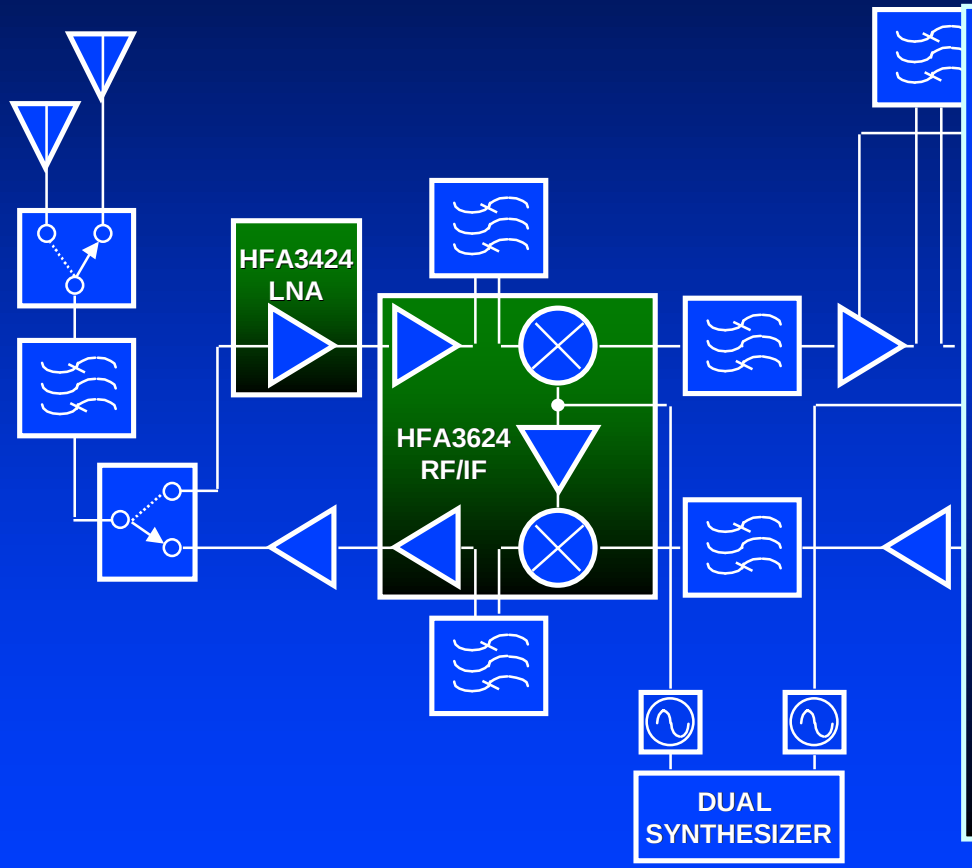
A Complete DS Spread Spectrum Radio Chipset



RF IC Partitioning Criteria

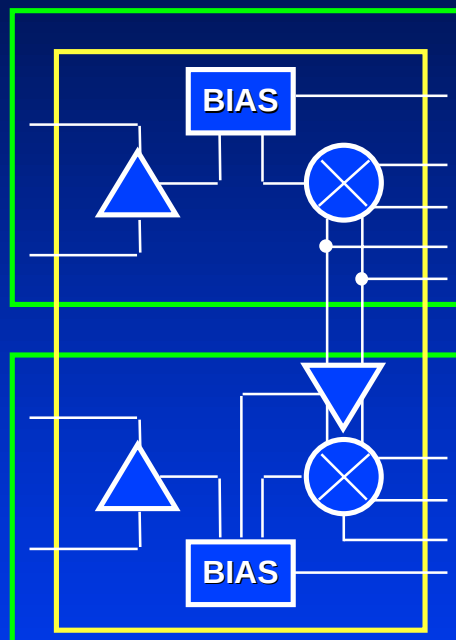
- FREQUENCY
- ANALOG / DIGITAL SIGNALS
- PROCESS TECHNOLOGY
- ISOLATION REQUIREMENTS
- POWER LEVELS
- PACKAGING
- EXTERNAL COMPONENTS

RF to IF Conversion Issues



- NOISE FIGURE (NF)
- INPUT/OUTPUT 1dB COMPRESSION POINT (IP1dB/OP1dB)
- INPUT/OUTPUT THIRD ORDER INTERCEPT POINT ($IP3_I$/ $IP3_O$)
- IMPEDANCE MATCHING
- DYNAMIC RANGE
- SPURIOUS FREE DYNAMIC RANGE (SFDR)

HFA3624 RF to IF Converter



Receive

- LNA
- SINGLE CONVERSION HETERODYNE MIXER

Transmit

- SINGLE CONVERSION MIXER
- LINEAR POWER PREAMP

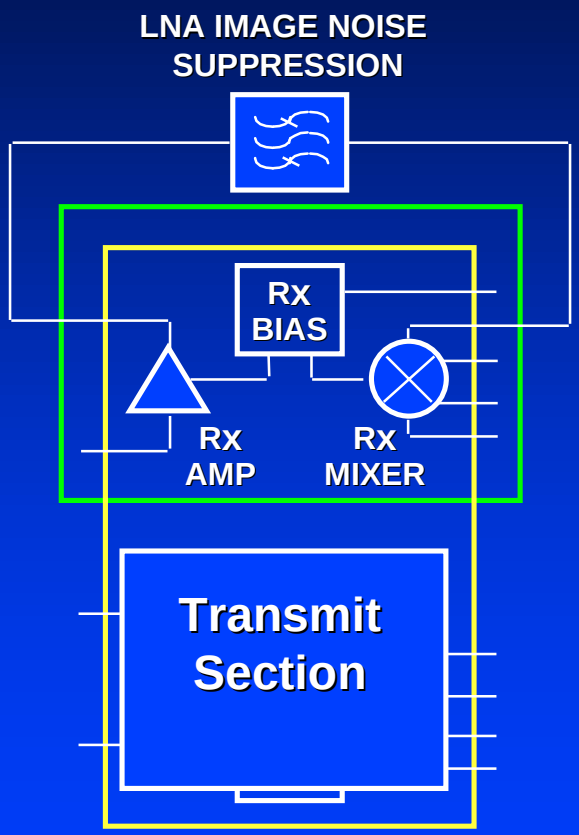
- INTEGRATED RECEIVE / TRANSMIT FRONT END
- 2.4 TO 2.5GHz RF FREQUENCY RANGE
- 10 TO 400MHz IF OPERATION
- SINGLE SUPPLY 2.7V TO 5.5V
- ALL RF I/Os MATCHED TO 50Ω
- INDEPENDENT RECEIVE / TRANSMIT POWER ENABLE

28-PIN SSOP

- 150mil WIDE
- 0.08 SQUARE INCHES

Rx	Tx	POWER CONSUMPTION
0	0	0.3µA
0	1	48mA
1	0	18mA

HFA3624 Receive Section



LNA @ 2.5GHz

- POWER GAIN 15.6dB
- OP1dB 5.5dBm
- NF 3.8dB

Mixer (LO = 2.15GHz)

- POWER CONVERSION GAIN 3.0dB
- $IP3_O$ 4.0dB
- NF 12.0dB

NF = 10LOG(F) = NOISE FIGURE
WHERE (F) = NOISE FACTOR
$F = SNR_I / SNR_O$

HFA3624 RF Front End Cascaded Performance

Cascaded Performance Data

- NF. 4.5dB
- IP1dB . . . . . -28dB
- $IP3_I$ . . . . . -18dB

Cascaded Performance Data

$$F_C = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots$$

- F_C = CASCADED NOISE FACTOR
- G_n = GAIN OF STAGE n

System Performance

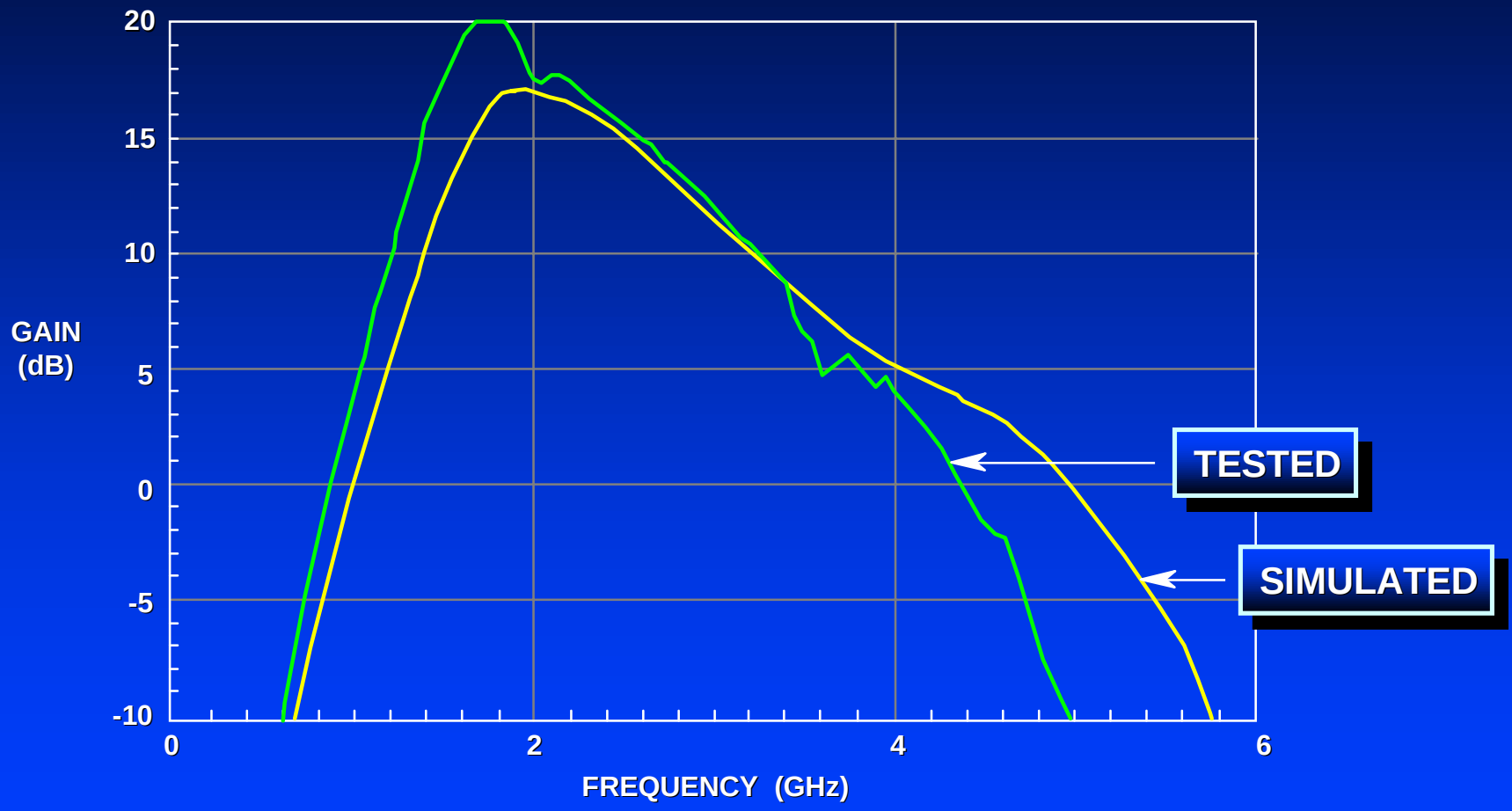
- DYNAMIC RANGE (IP1dB - MDS)
- SPURIOUS FREE DYNAMIC RANGE
  $2/3(IP3_I - MDS)$

F_c Effect on Sensitivity (MDS)

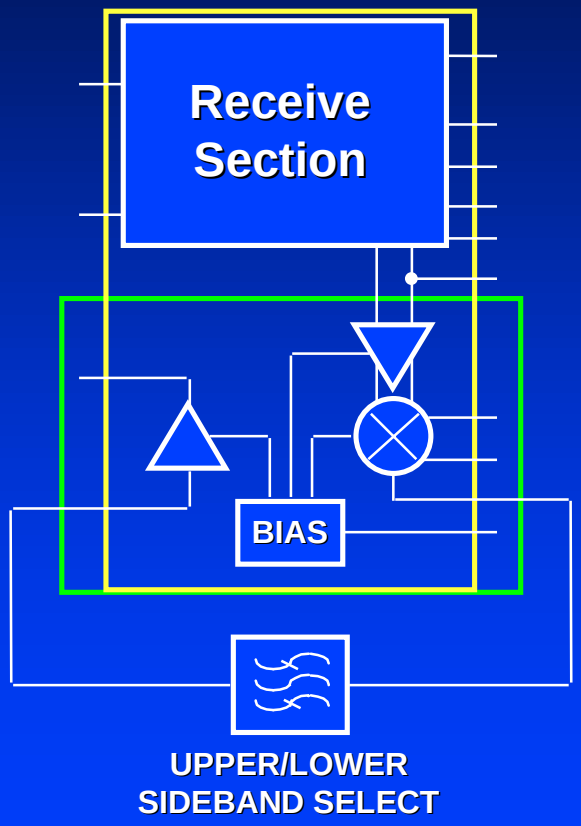
- $MDS = F_C(kTB)\ (SNR)_O$

where: MDS = Minimum Discernible Signal
k = Boltzmann's Constant
T = Absolute Temperature in Kelvin
B = Bandwidth
$(SNR)_O$ = Output Signal-to-Noise Ratio

HFA3624 Receive Amplifier Power Gain (S21)



HFA3624 Transmit Section



Mixer (Upconverter)

- POWER CONVERSION GAIN 5.8dB
- LO LEAKAGE . . . . . -20.0dB

Pre-Amp

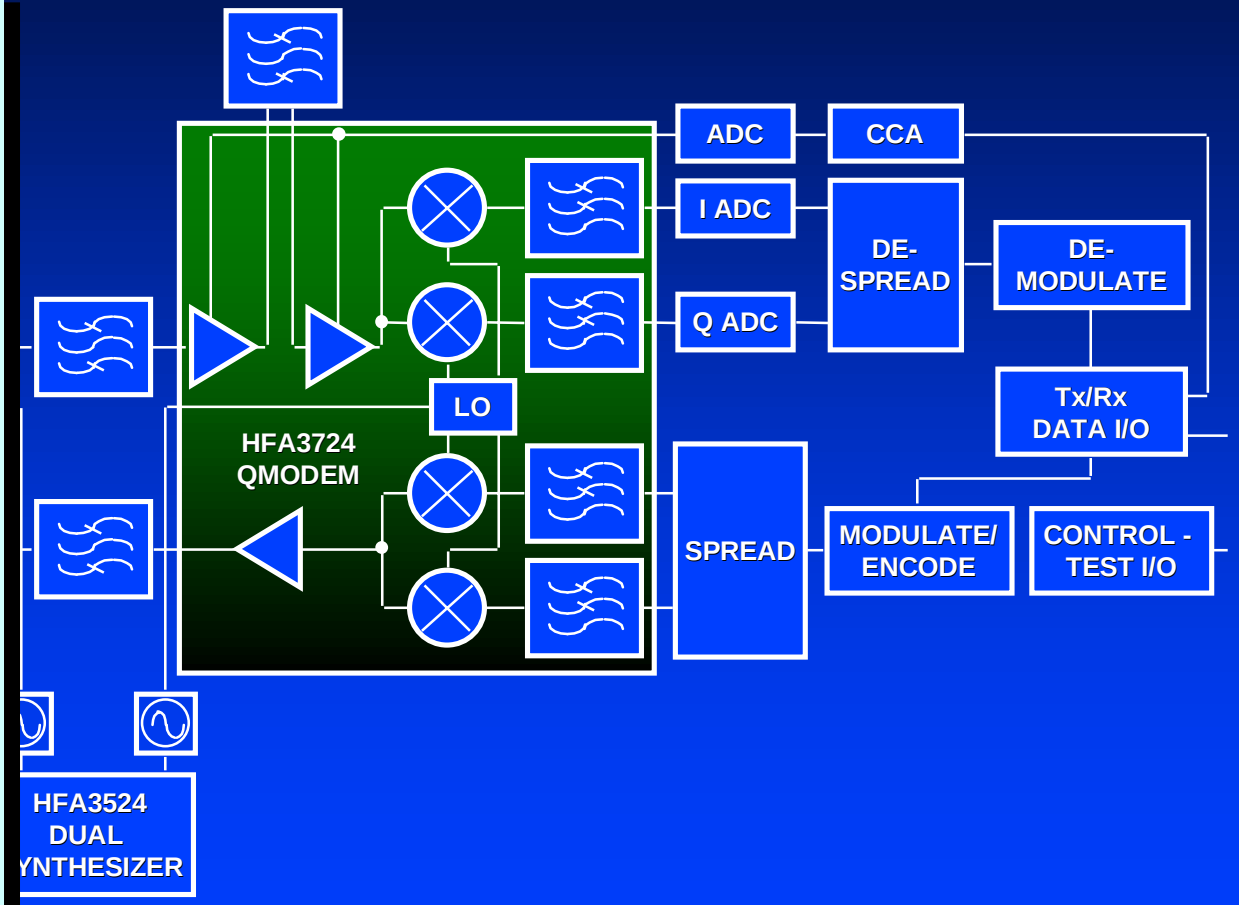
- POWER GAIN 13.0dB
- OP1dB . . . . . +7.5dBm

Cascaded Performance

- POWER GAIN 17.8dB
- OP1dB 0.5dBm
- LO LEAKAGE . . . . . -5.0dBm

IF to Baseband Conversion Issues

- PRIMARY SOURCE OF GAIN
  - Limiter or AGC
- RSSI TO MEASURE INPUT SIGNAL
- COMPLEX DOWN CONVERSION TO BASEBAND
- QUADRATURE LO GENERATION
- FILTERING (BASEBAND)
  - Anti-aliasing on Receive
  - Pulse Shaping on Transmit
- UP CONVERSION / MODULATION
- POWER SAVING FEATURES



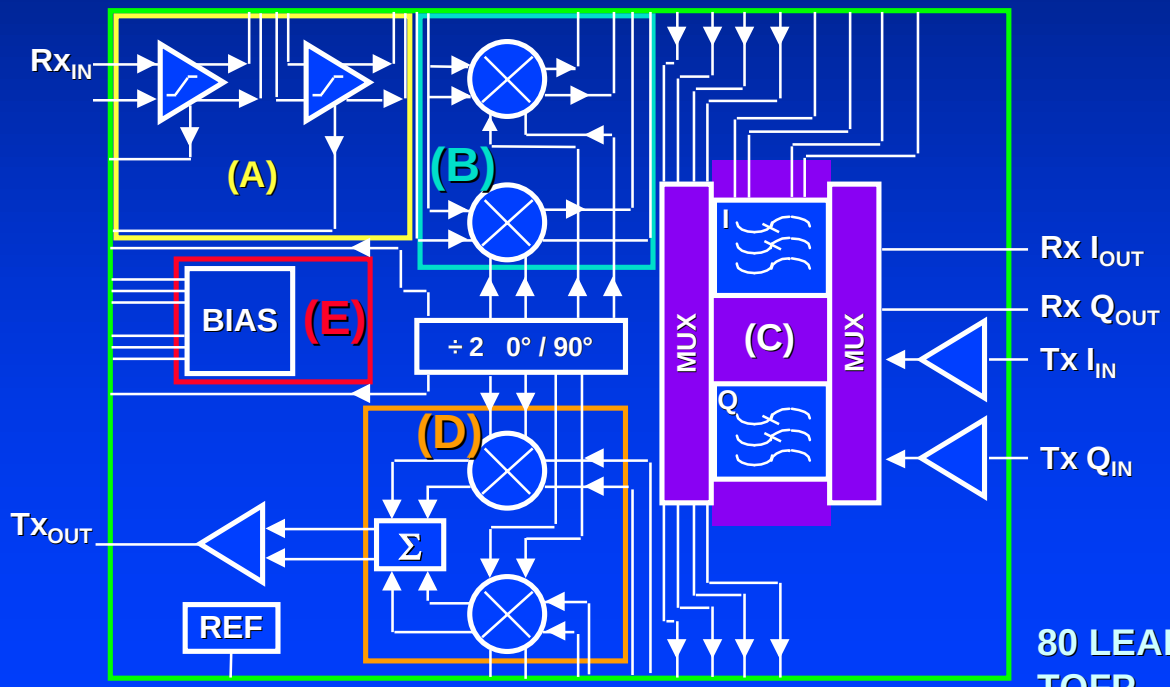
HFA3724 Quadrature IF Modulator / Demodulator

(A) Limiter and RSSI

- IF UP TO 400MHz
- 84dB GAIN
- 70dB RSSI DYNAMIC RANGE

(B) Demodulator

- DOWN CONVERTS 10 TO 400MHz IF TO BASEBAND
- IN PHASE (I) AND QUADRATURE (Q)



80 LEAD TQFP

(C) Filter

- TWO LOW PASS FILTERS (I AND Q)
- DIGITALLY SELECTABLE FILTER CUTOFF
- MULTIPLEXED RECEIVE / TRANSMIT

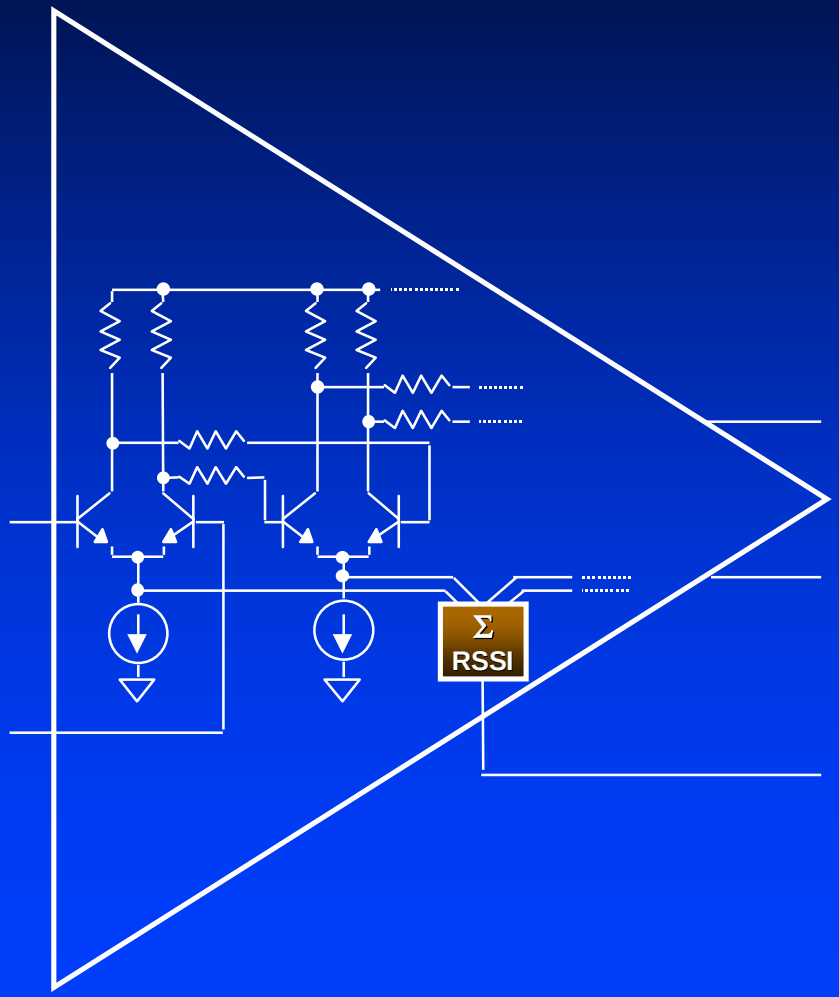
(D) Modulator

- UP CONVERT AND PHASE MODULATES I AND Q TO 300MHz

(E) Power

- POWER CONTROL INCORPORATING SLEEP MODE
- HALF DUPLEX OPERATION

HFA3724 Limiter and RSSI



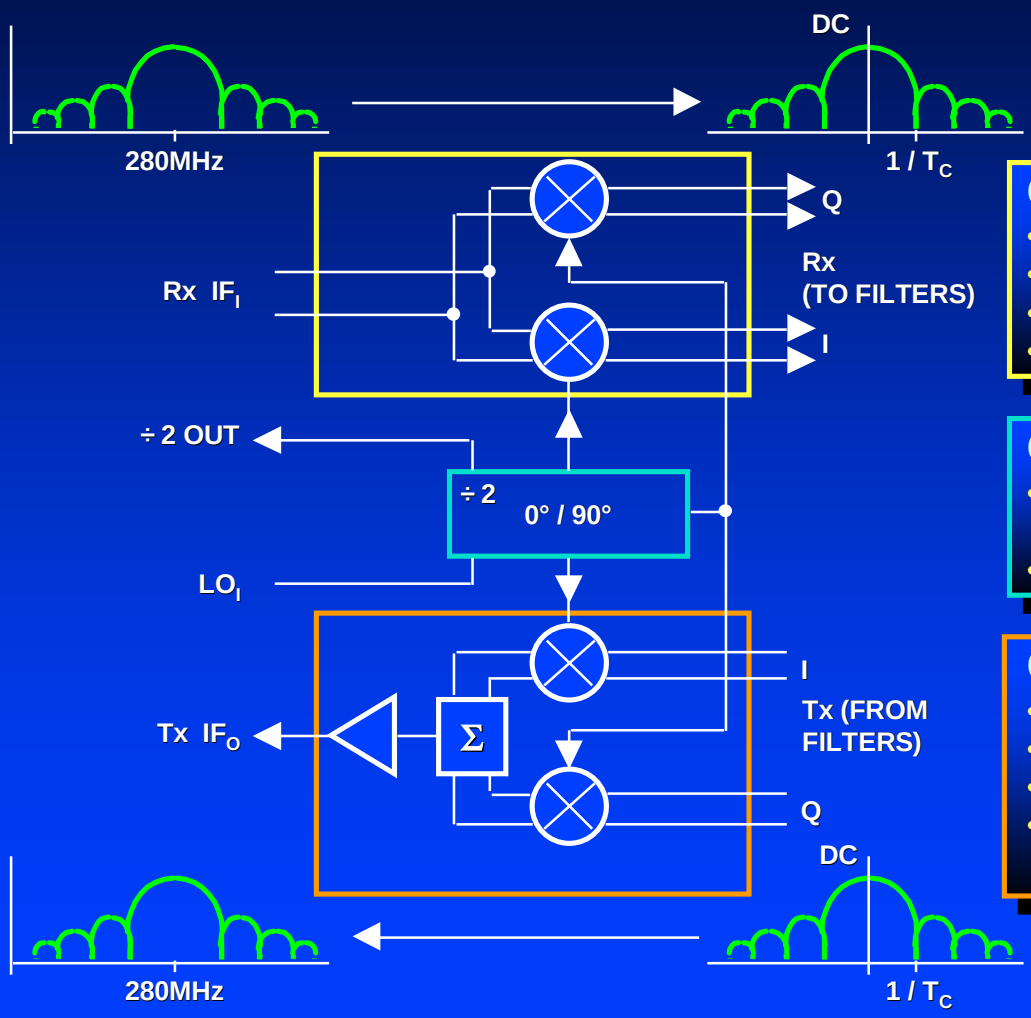
Limiter

- TWO INDEPENDENT AMPLIFIERS
- GAIN (EACH AMP)
  FROM 10 TO 400MHz 42dB
- LIMITER -3dB
  SENSITIVITY. . . . . -84dBm
- NF (FOR 250Ω SINGLE ENDED
  INPUT IMPEDANCE) 6dB

RSSI

- SENSITIVITY. . . . . -84dBm
- DYNAMIC RANGE 70dB
- RSSI SLOPE 5μA/dB

HFA3724 Q-Modem



Quadrature Downconverter

- INPUT FREQUENCY RESPONSE 400MHz
- DIFFERENTIAL VOLTAGE GAIN 8dB
- PHASE MATCH . . . . . ±2°
- AMPLITUDE MATCH . . . . . ±0.5dB

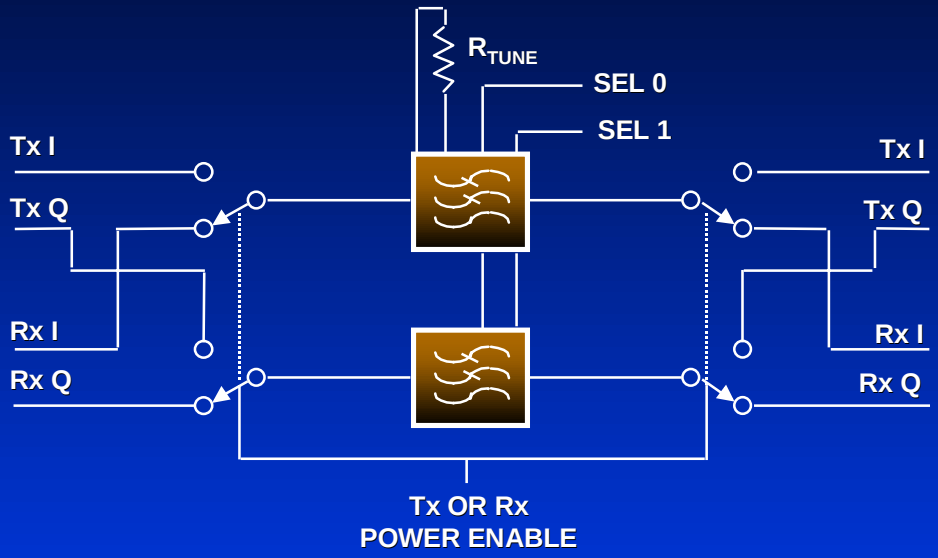
Quadrature LO Generator

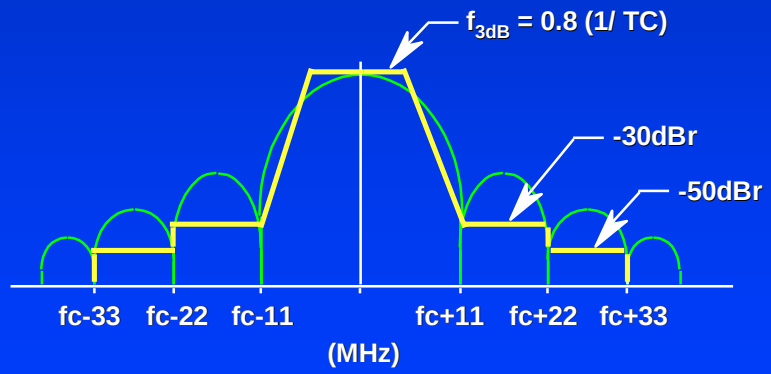
- INTERNAL DIVIDE BY 2 FLIP-FLOP WITH DUTY CYCLE COMPENSATION
- 50Ω DIVIDED BUFFER OUTPUT AVAILABLE

Quadrature Upconverter

- PHASE MATCH . . . . . ±2°
- AMPLITUDE MATCH . . . . . ±0.5dB
- LO LEAKAGE . . . . . -30dBc
- MINIMUM SIDEBAND SUPPRESSION (400MHz) 26dBc

HFA3724 Baseband Filters



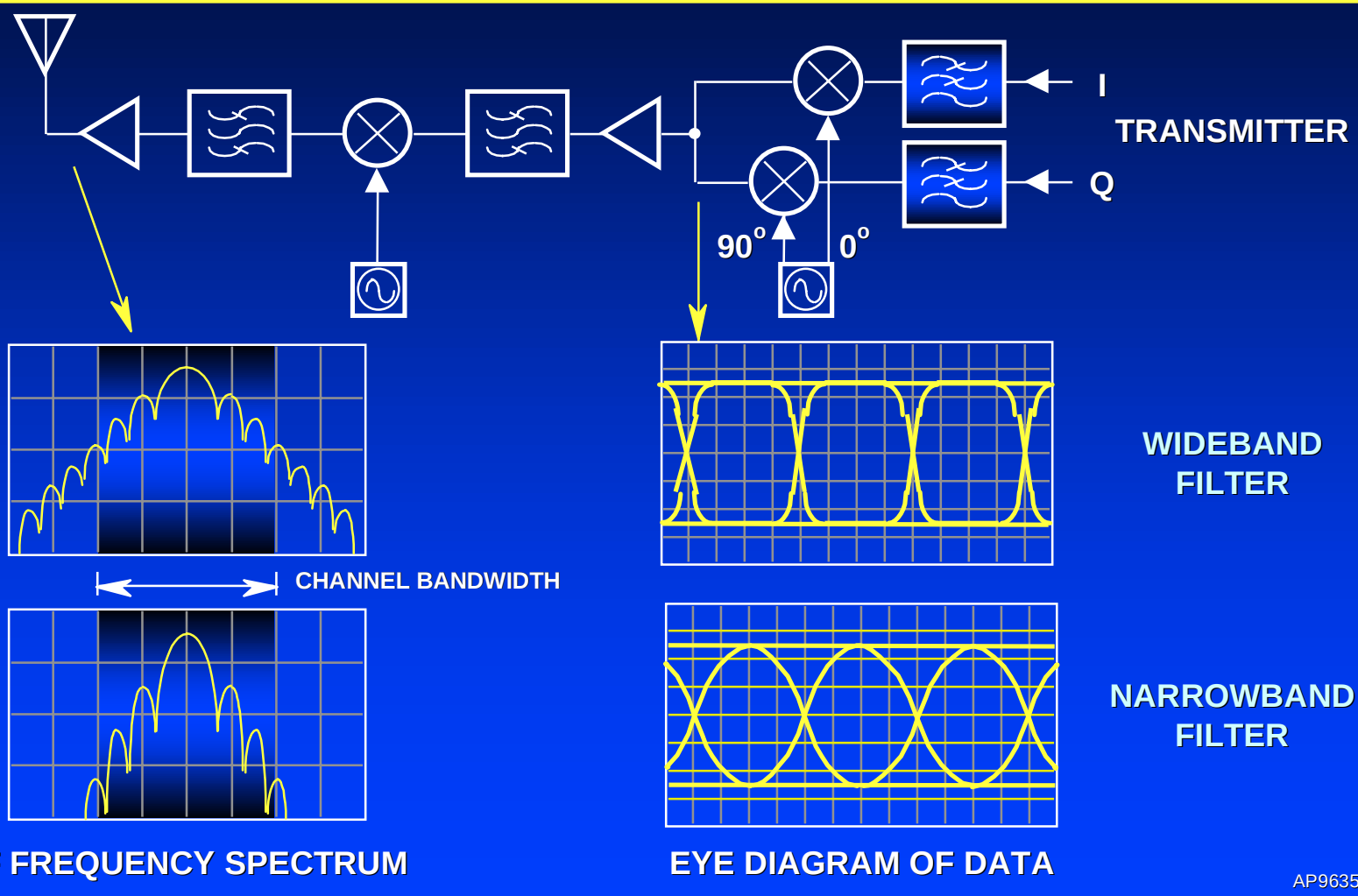


802.11 SPECTRAL MASK

- 5 - POLE BUTTERWORTH FILTERS
- MULTIPLEXED FILTERS FOR HALF DUPLEX OPERATION
  - Pulse Shaping on Transmit
  - Anti-aliasing on Receive
- FOUR SELECTABLE CUTOFF
- FREQUENCIES: 2.2MHz, 4.4MHz, 8.8MHz, 17.6MHz
- ± 20% FINE TUNING WITH EXTERNAL RESISTOR

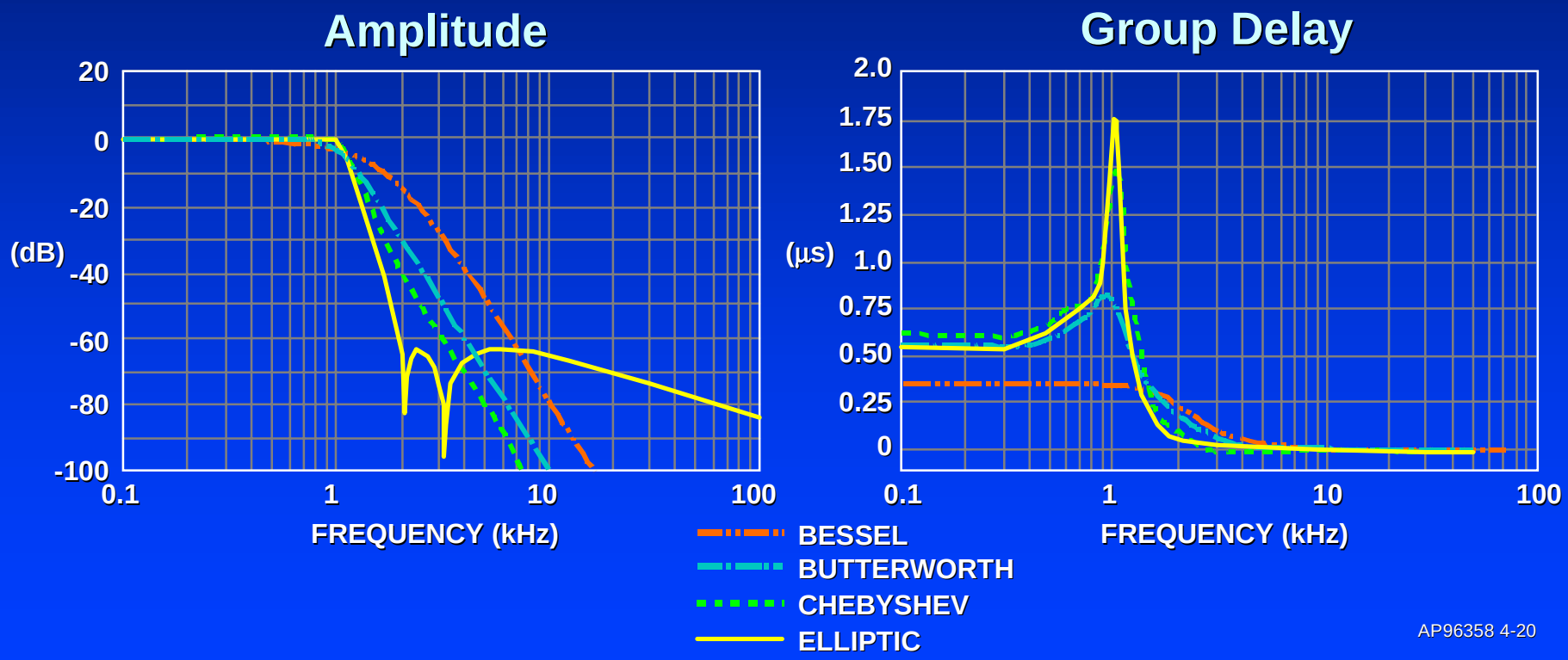
- TRANSMIT FILTERING REDUCES SPECTRAL PRODUCTS TO IEEE802.11 SPECIFIED LEVELS
- TUNING RESISTOR COMPENSATES FOR SPECTRAL RE-GROWTH

Adjacent Channel Interference Versus Intersymbol Interference



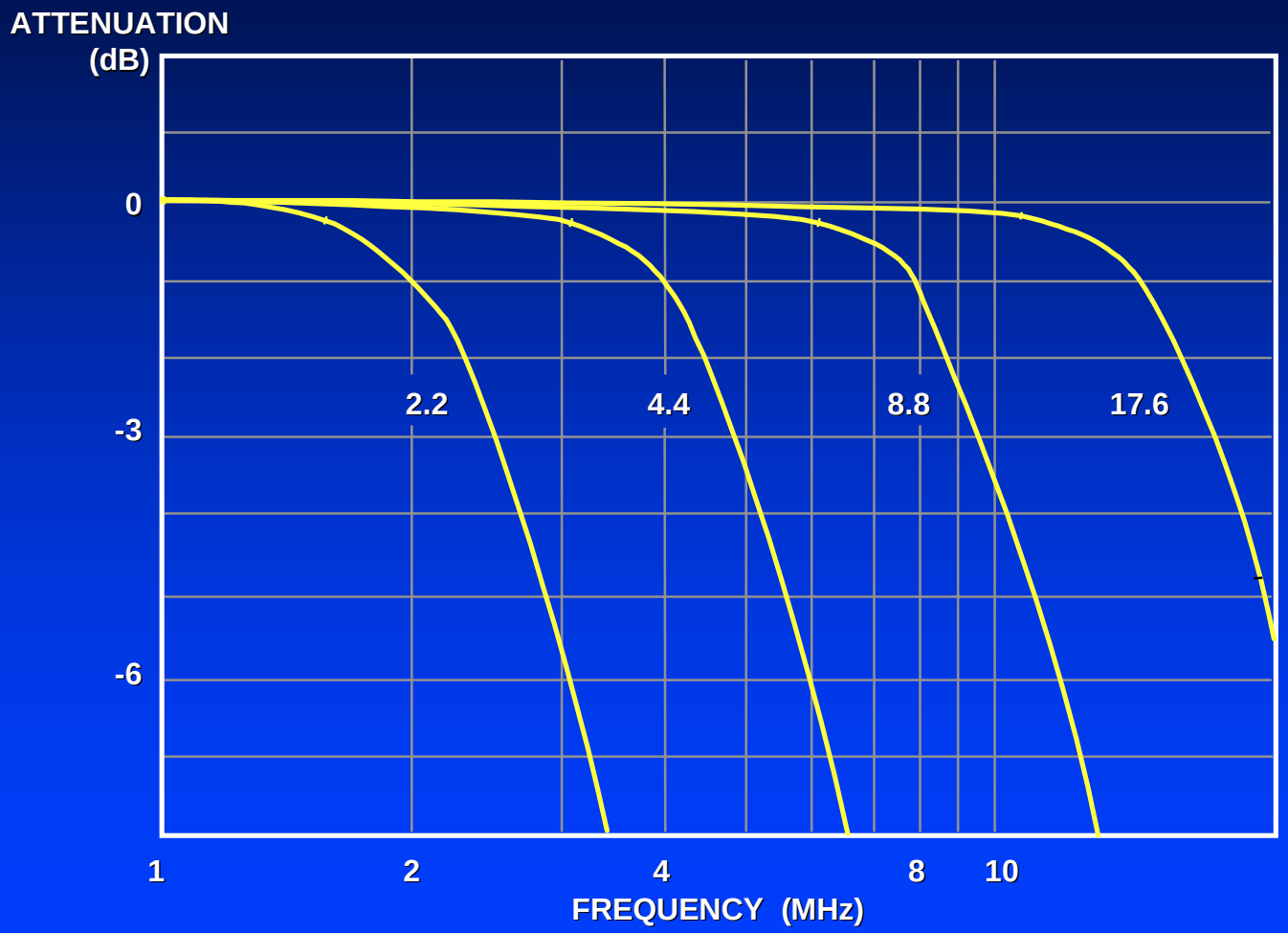
Filter Response Comparison

- THEORETICAL AMPLITUDE AND GROUP DELAY OF FOUR DIFFERENT FILTERS
- FILTERS ARE 5 POLE
- CUTOFF FREQUENCY NORMALIZED TO 1kHz



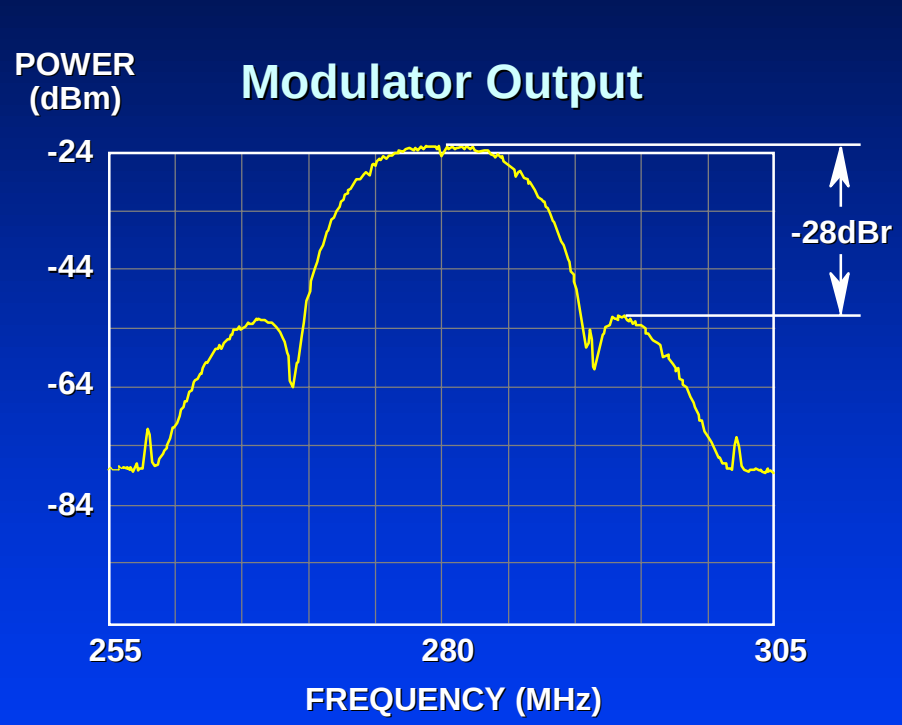
AP96358 4-20

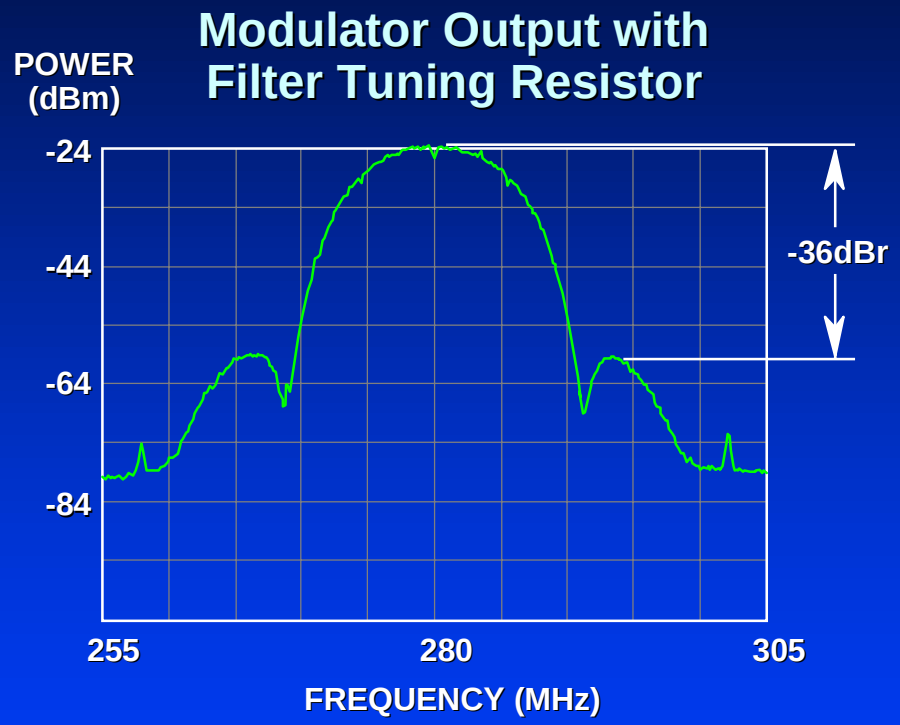
Filter Cutoff Frequency Selection



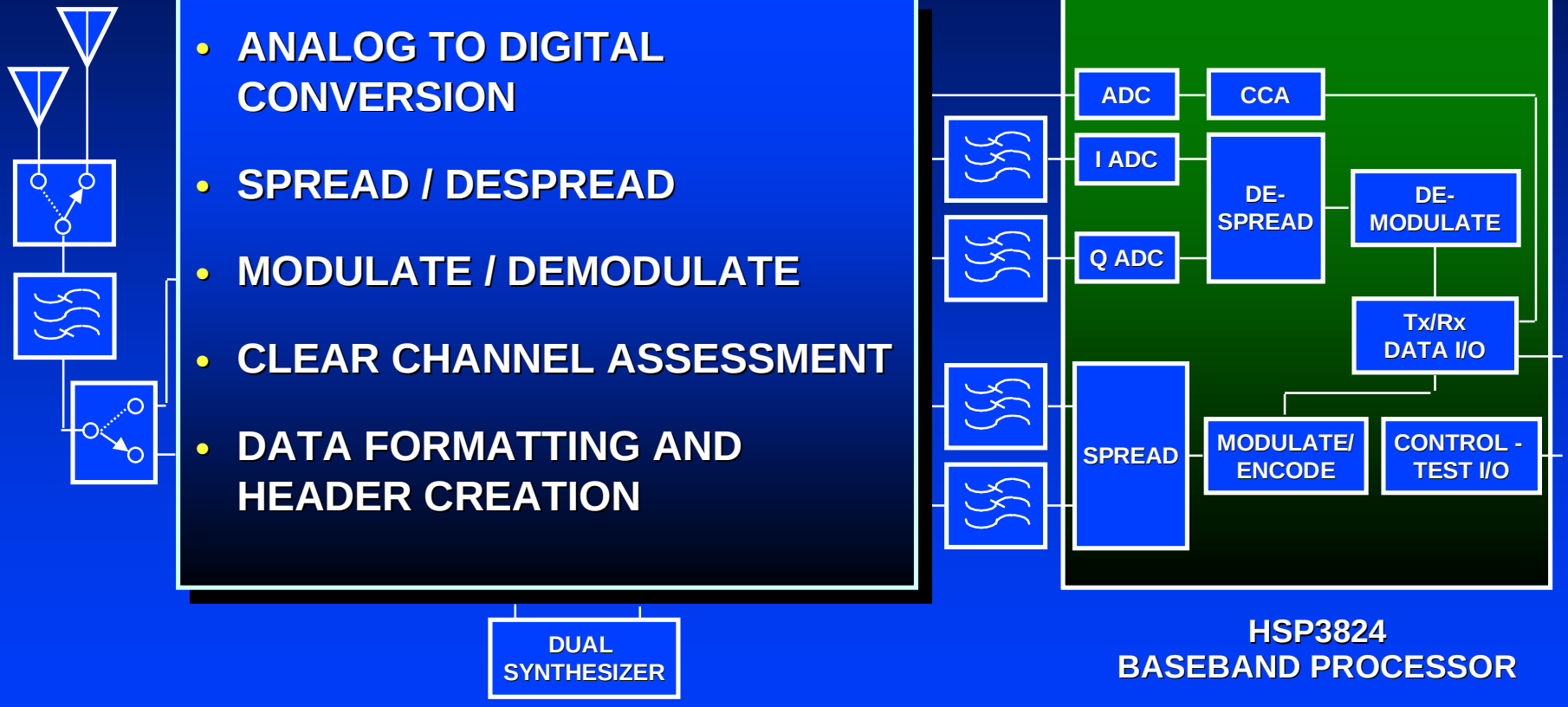
SEL 1	SEL 0	f_{3dB} (MHz)
0	0	2.2
0	1	4.4
1	0	8.8
1	1	17.6

HFA3724 Performance Data

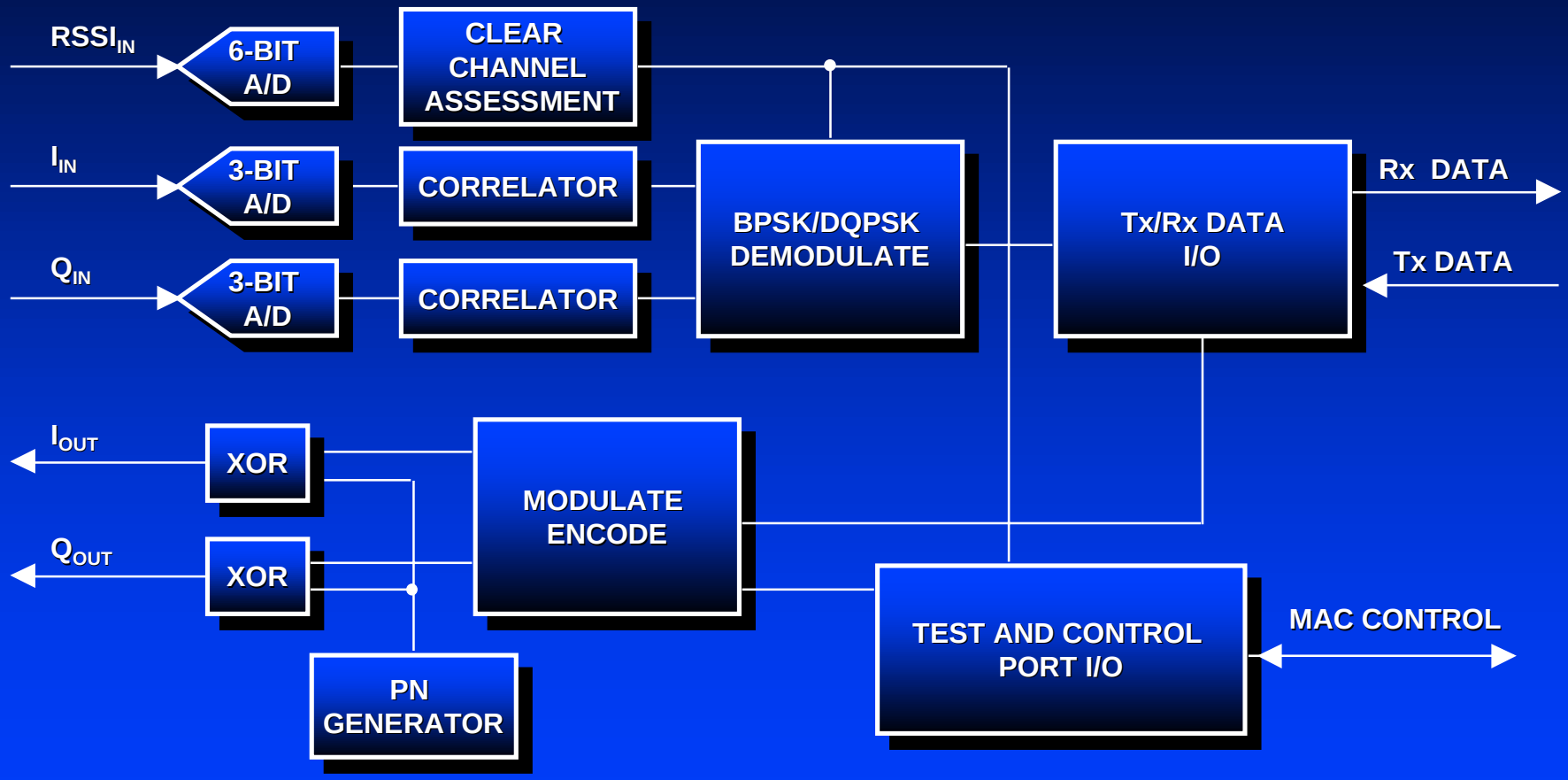




Baseband Section Issues

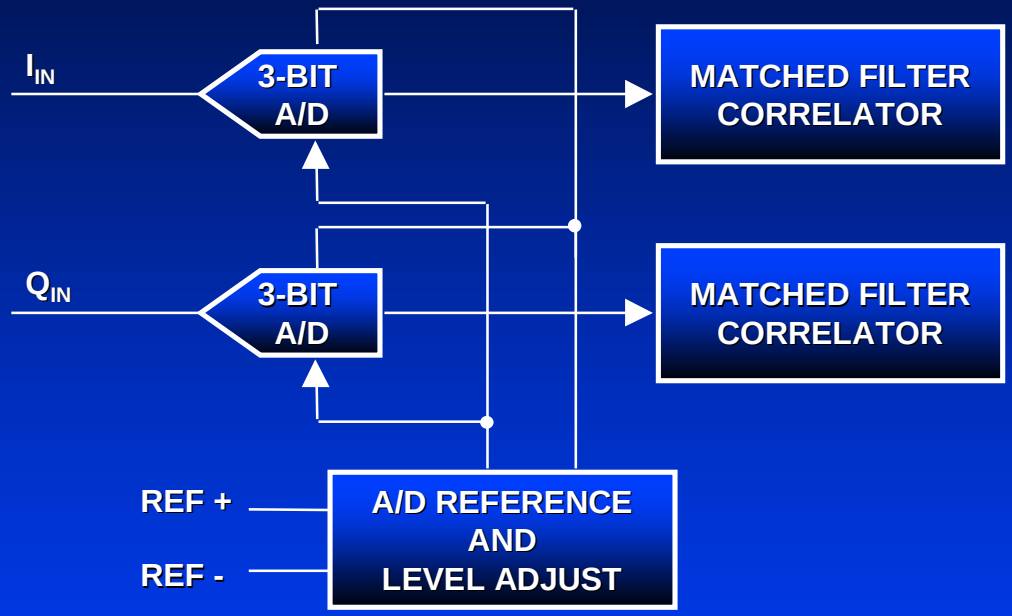


HSP3824 Baseband Processor



HSP3824 Analog to Digital Converters

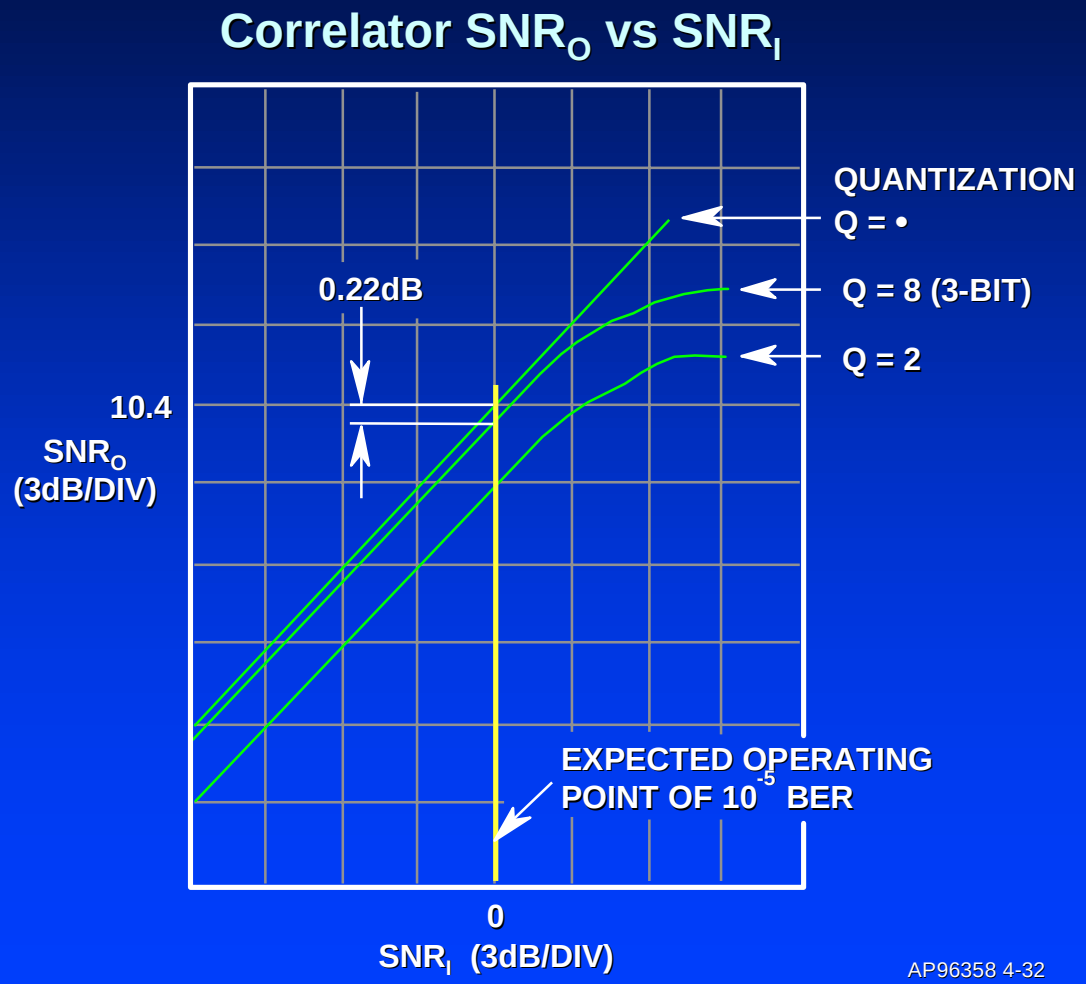
- 44Msps, 3-BIT FLASH A/Ds SAMPLE I/Q INPUTS
- PATENTED CIRCUITRY ACTS AS AGC TO KEEP A/Ds AT FULL SCALE



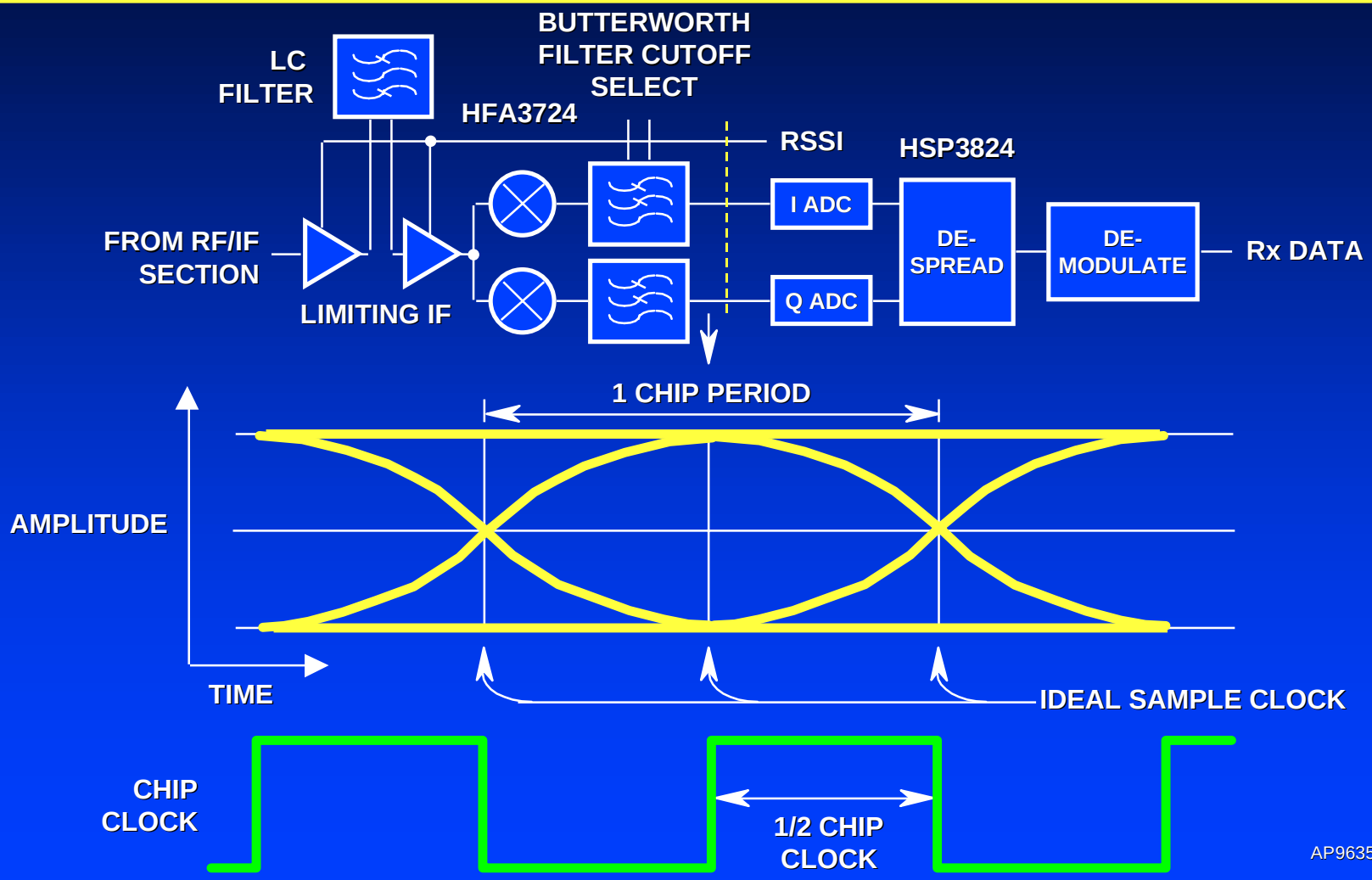
- 2Msps, 6-BIT A/D SAMPLES RSSI

Why 3-Bits?

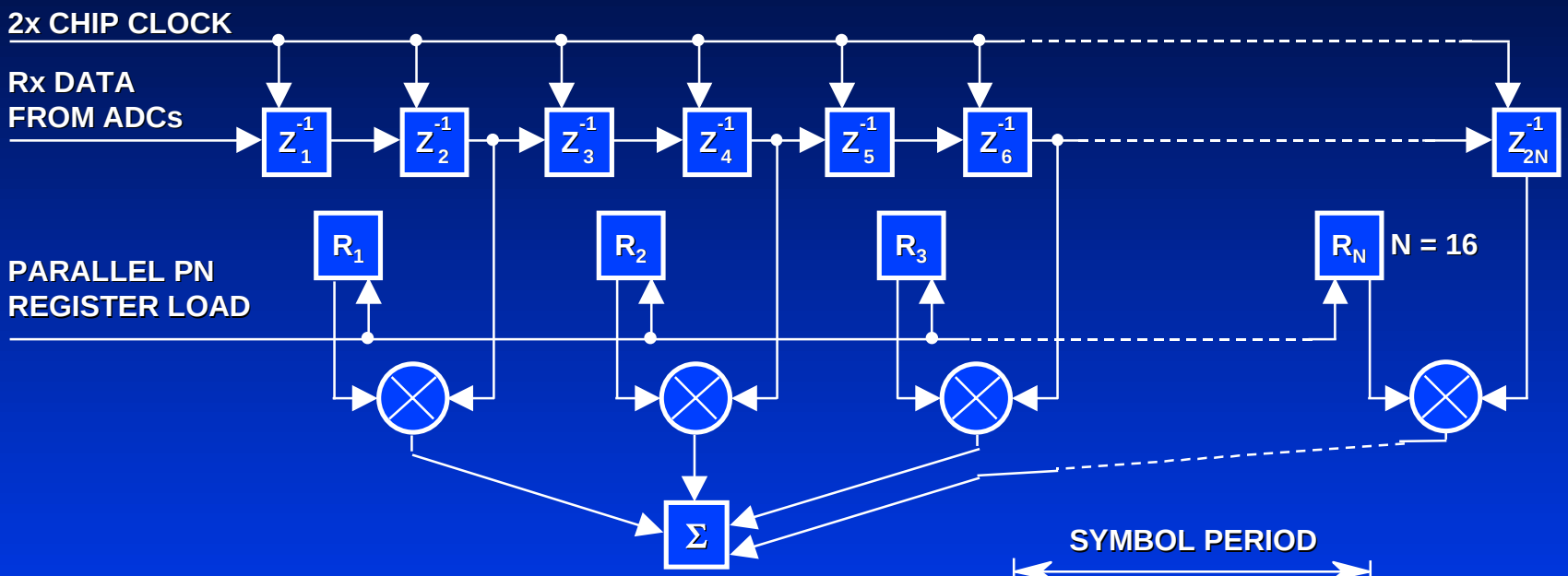
- 3-BIT QUANTIZATION GIVES SIGNIFICANT ADVANTAGE OVER 1-BIT
- QUANTIZATION TO GREATER THAN 3-BITS YIELDS NEGLIGIBLE IMPROVEMENT



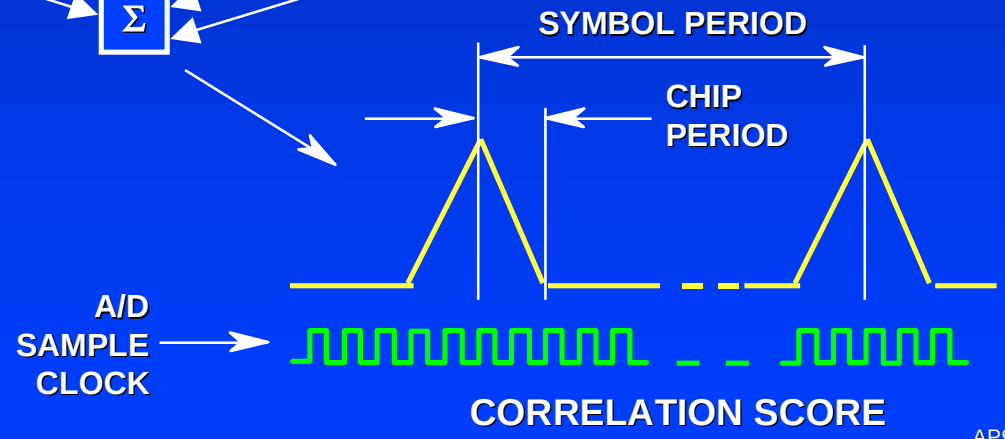
Sample Clock Timing



HSP3824 Matched Filter Correlator

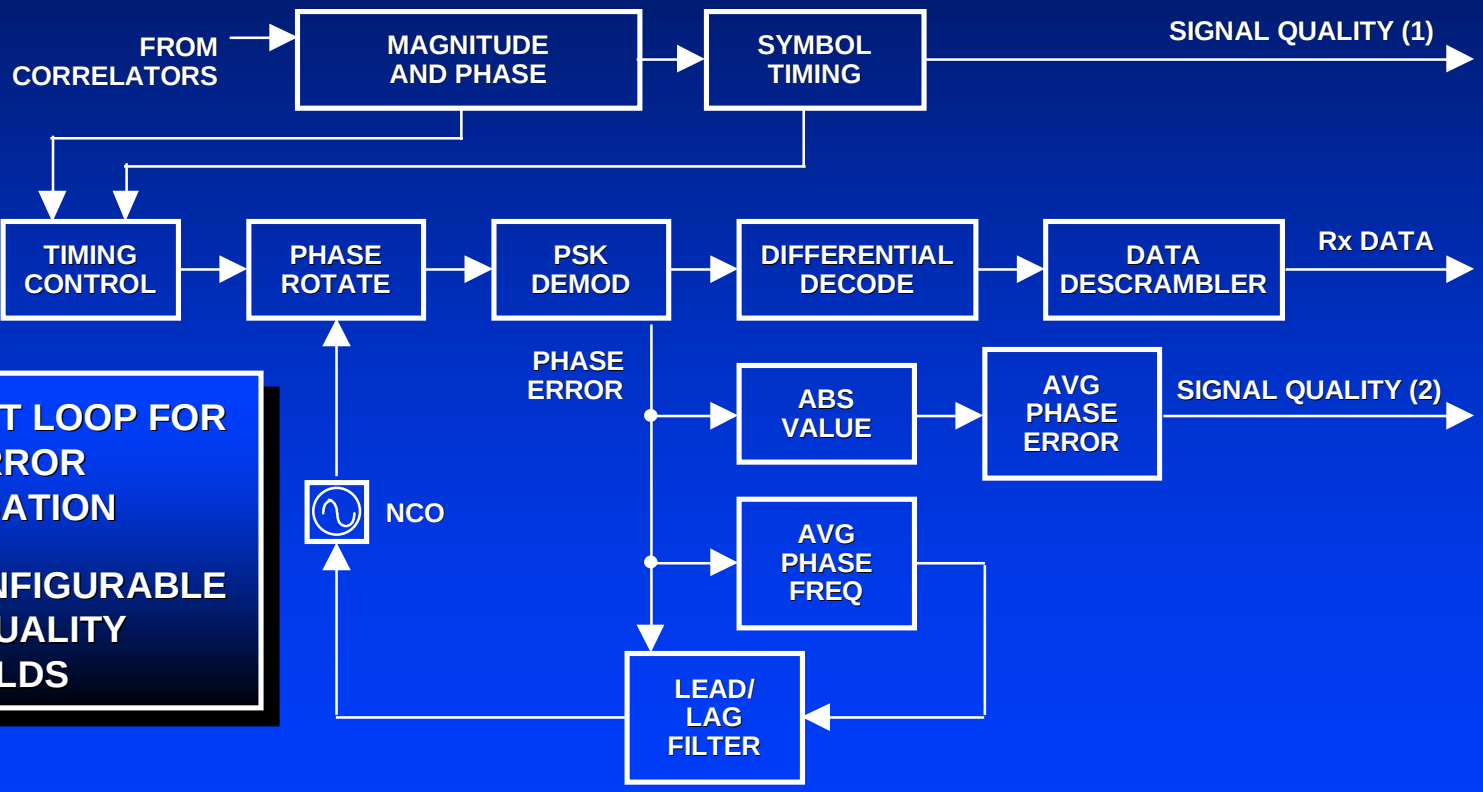


11-BIT BARKER CODE EXAMPLE:
+1 -1 +1 +1 -1 +1 +1 +1 -1 -1 -1



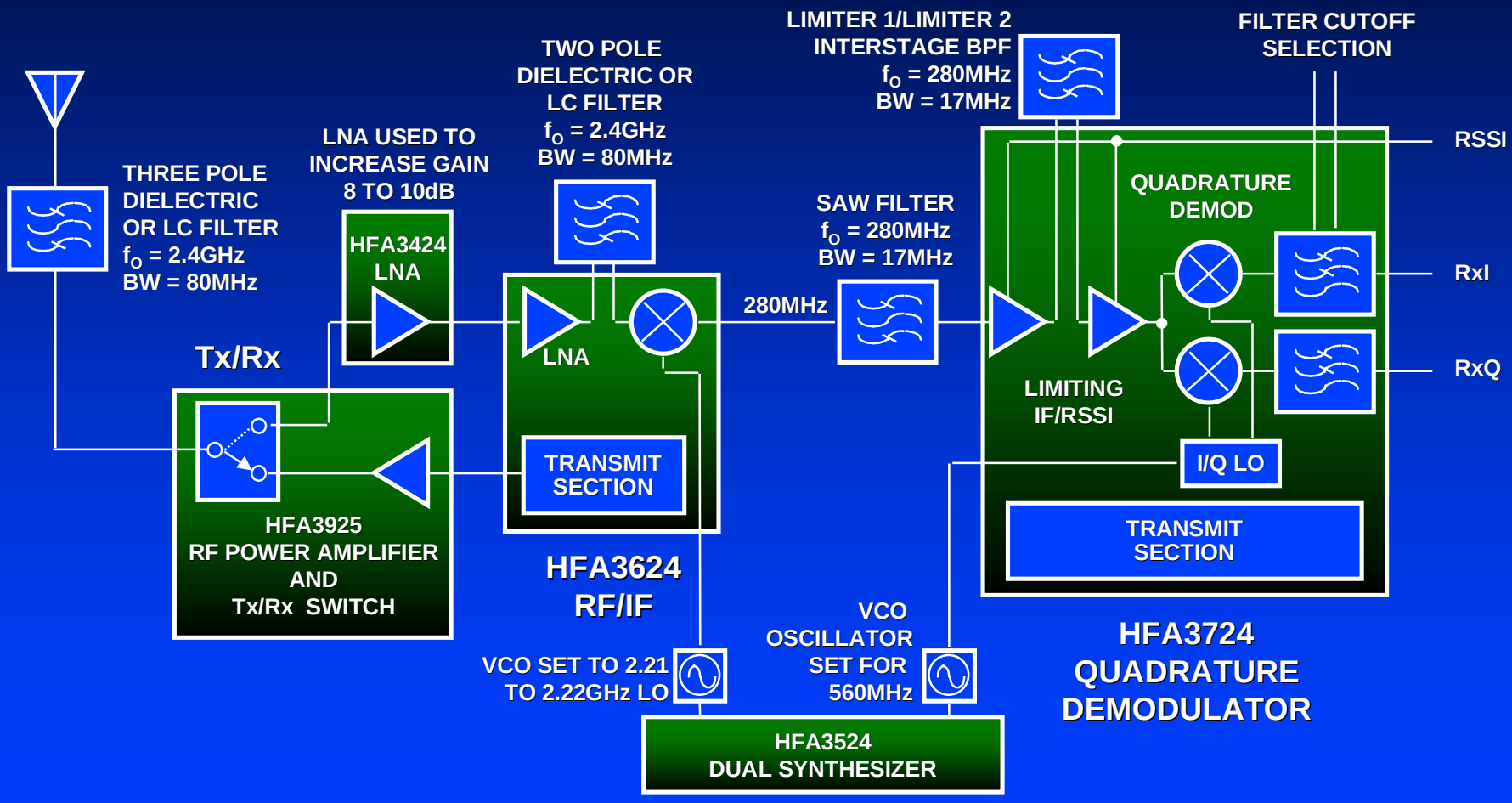
HSP3824 Receive Section

DPSK Demodulator

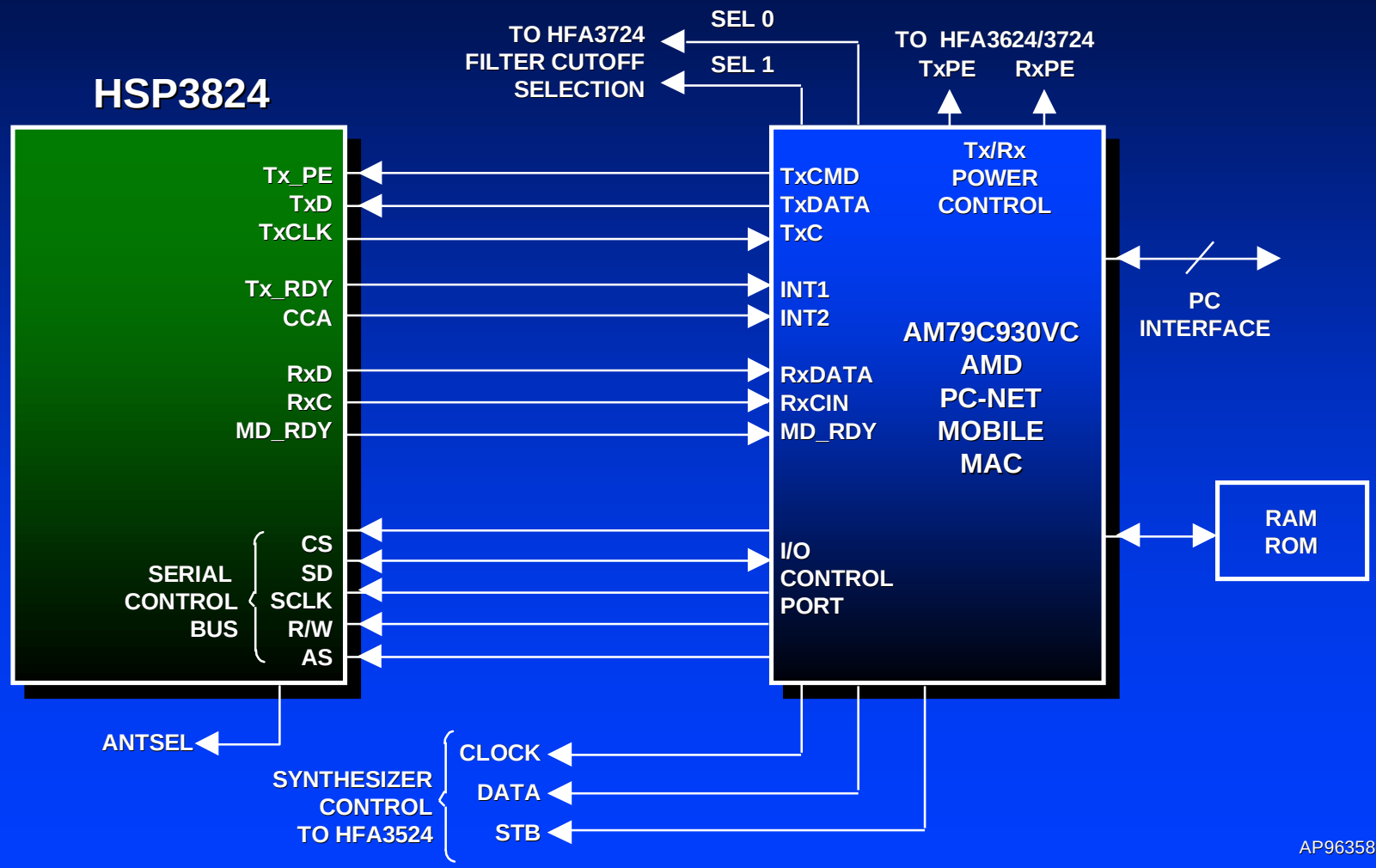


- COHERENT LOOP FOR PHASE ERROR COMPENSATION
- USER CONFIGURABLE SIGNAL QUALITY THRESHOLDS

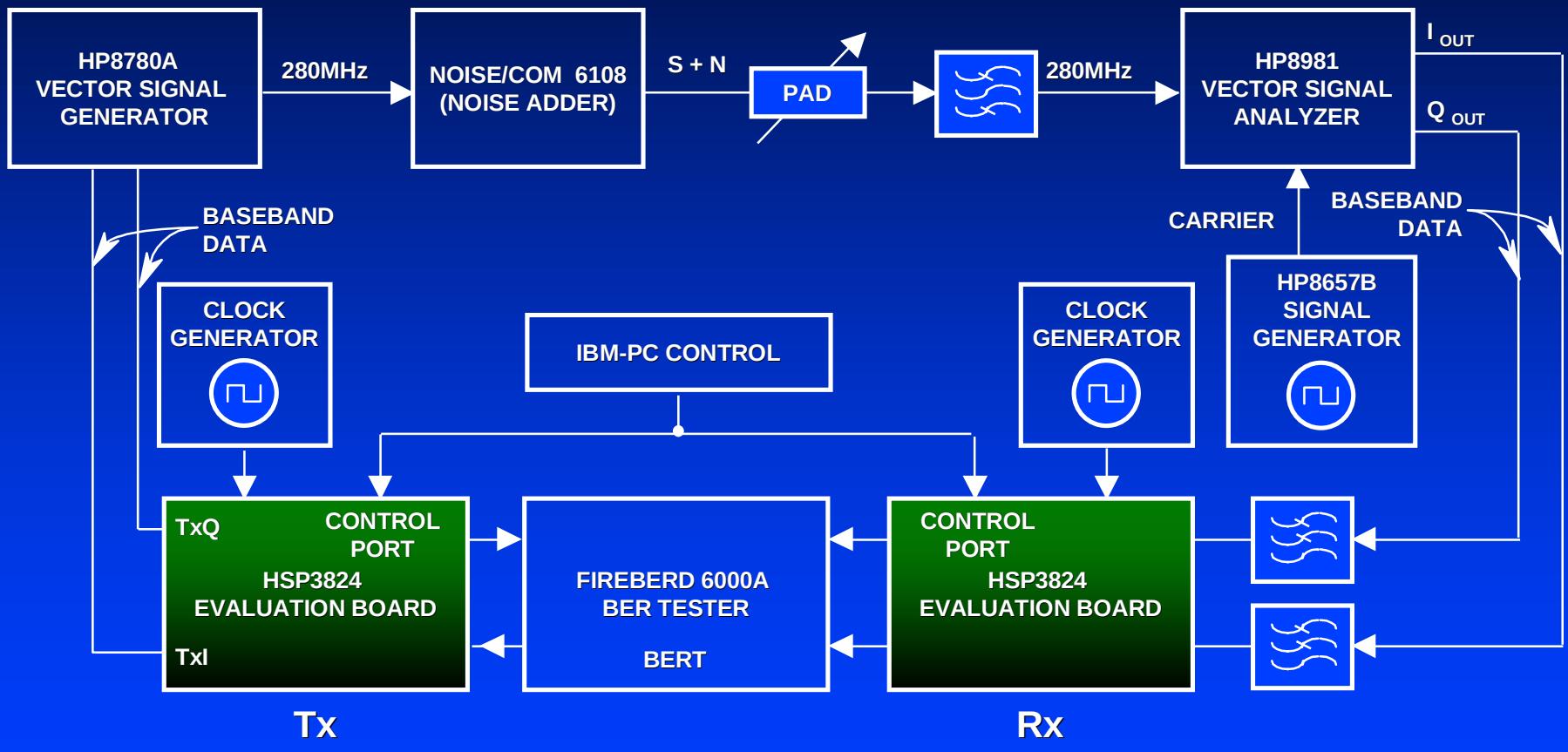
Complete RF to Baseband Circuit



MAC-PHY Glueless Interface



HSP3824 Evaluation Setup

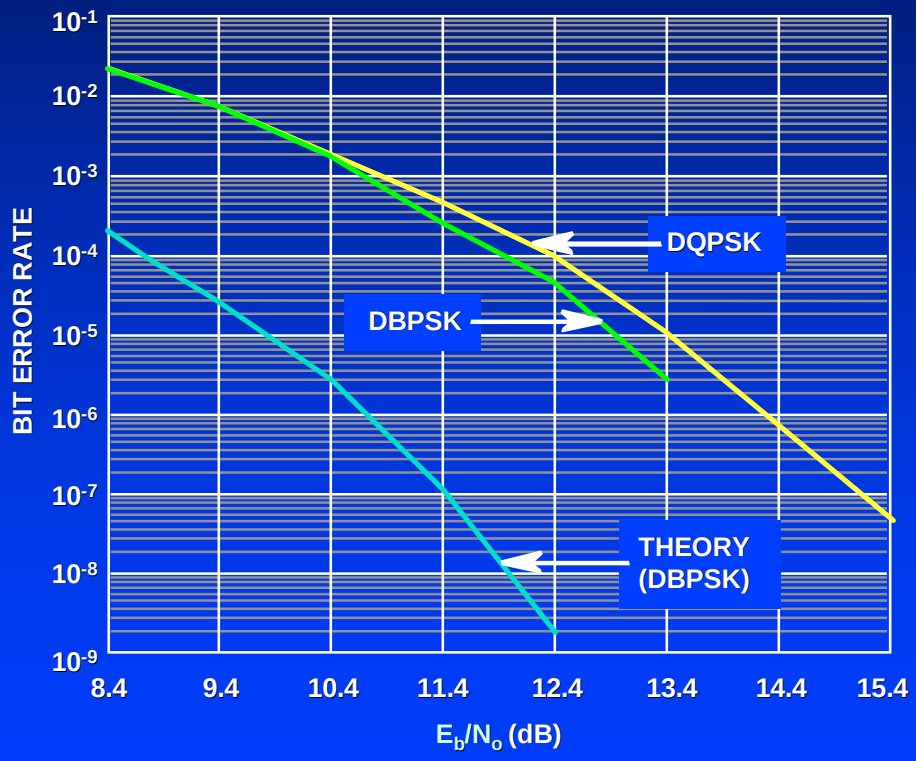


BER Performance

PARAMETER	LOSS IN dB @ 10^{-5} BER
PHASE NOISE	*
LIMITING AMPLIFIERS IN IF	0.5
I/Q PHASE AND AMPLITUDE IMBALANCE	0.75
A/D LINEARITY	NEGLIGIBLE
A/D HEADROOM vs BIAS ADJUSTMENT	NEGLIGIBLE
OSCILLATOR OFFSET IN CORRELATOR AT 50ppm	0.22
SAMPLING STRADDLING OFFSET AND IF + LPF FILTER LOSSES	2.0
QUANTIZATION AND DQPSK DEMOD LOSS	0.5
PHASE LOCK LOOP NOISE	0.1
DESCRAMBLER ERROR EXTENSION	0.5

* Depends on synthesiser

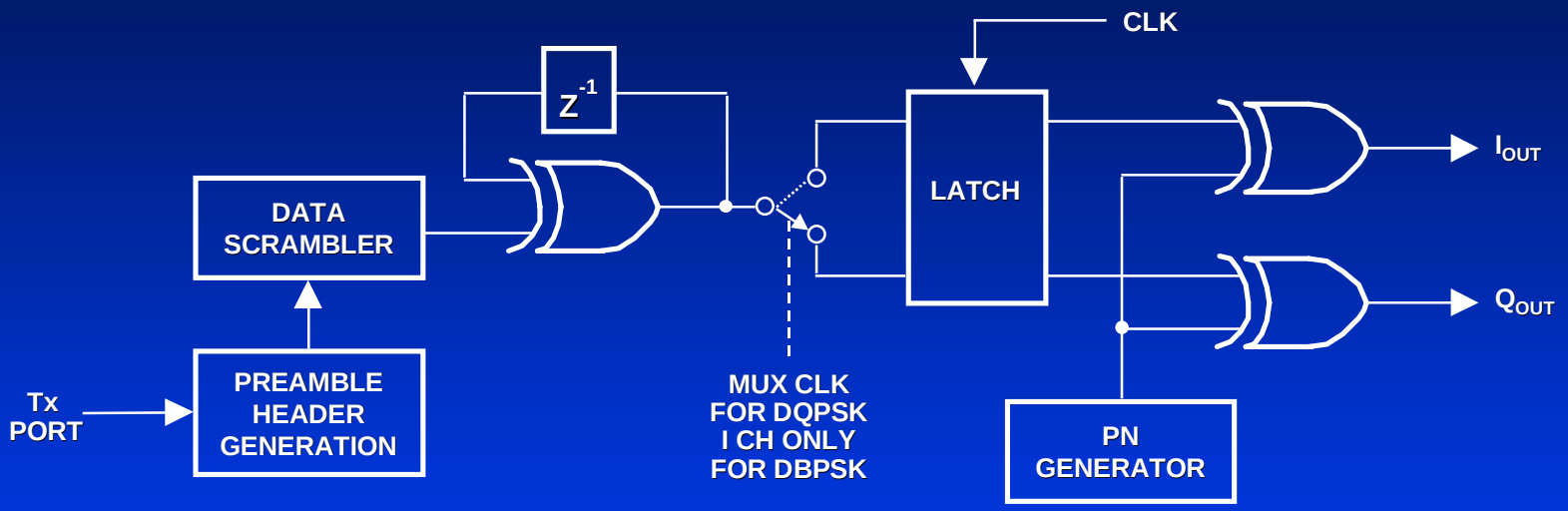
BER vs E_b/N_o Performance



AP96358 4-41

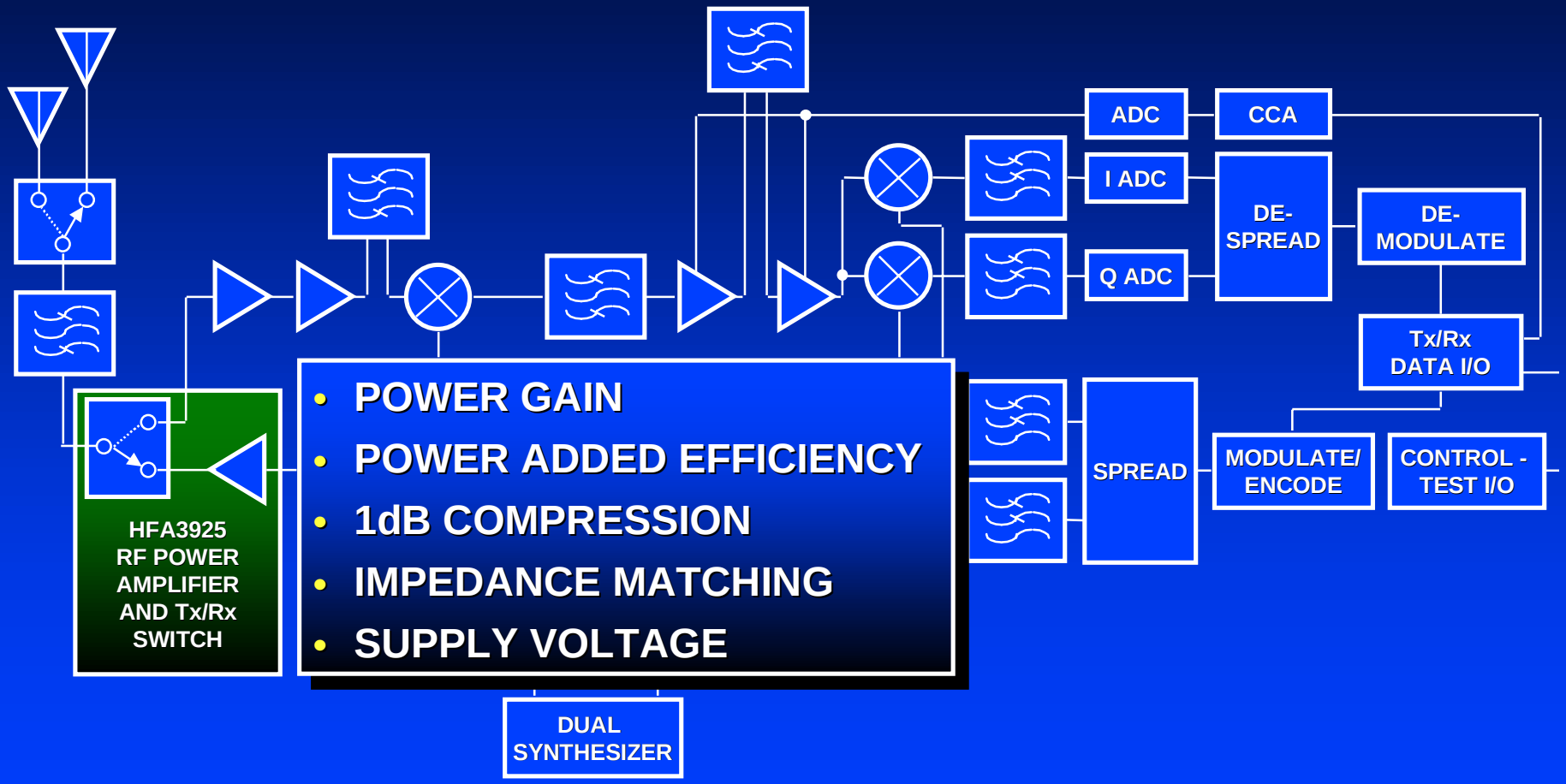
HSP3824 Transmit Section

DPSK Modulator

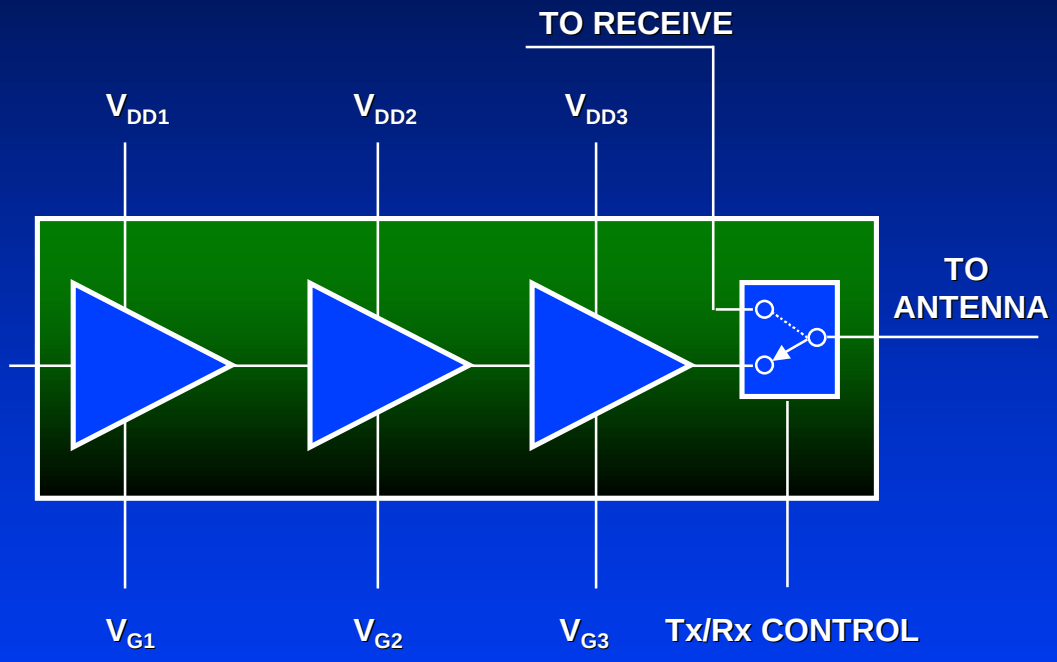


- FOUR SELECTABLE, INTERNALLY GENERATED PREAMBLE/HEADER FORMATS
- SELECTABLE CHIP SEQUENCES OF 11, 13, 15 OR 16 CHIPS PER SYMBOL
- SYMBOL RATE = MCLK/(N * CHIPS PER SYMBOL)
  WHERE MCLK = SAMPLE RATE CLOCK AND N IS A PROGRAMMABLE DIVIDER OF 2, 4, 8 OR 16

RF Power Amplifier Issues



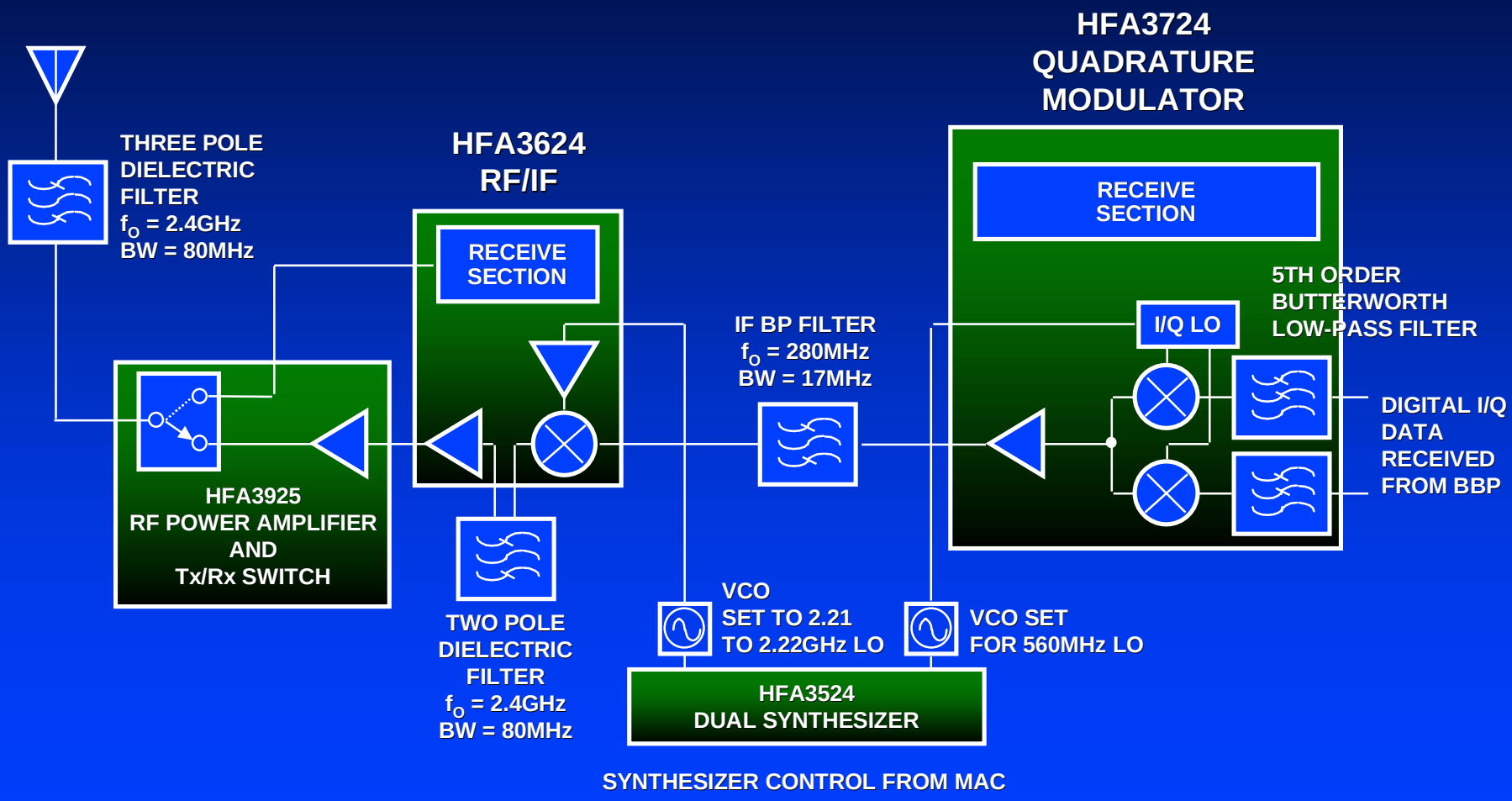
HFA3925 RF Power Amplifier and Switch



28 Lead SSOP

- HIGHLY INTEGRATED GaAs POWER AMPLIFIER WITH T/R SWITCH
- HIGH LINEAR OUTPUT POWER AT OP1dB 24dBm (250mW)
- INDIVIDUAL GATE CONTROL FOR EACH AMPLIFIER STAGE
- VSWR IN/OUT 1.75:1
- SUPPLY VOLTAGE . . . 2.7 TO 6V
- T/R SWITCH
  - Insertion Loss 1.2dB
  - Isolation 12dB

Complete Baseband to RF Circuit



SOFTWARE RADIOS

- PROGRAMMABLE RADIOS TO ACCOMODATE VARIOUS MODULATION REQUIREMENTS.
- DIGITAL SIGNAL PROCESSING TECHNIQUES.
- DIGITAL FILTERING TECHNIQUES.

Summary of Cellular and PCS Standards

IS-95
CDMA/FDM 1.25MHz BW
20 Chs BPSK/OQPSK
798 Users/Ch

GSM
TDMA/FDM 200kHz BW
124 Chs GMSK
8 Users/Ch

AMPS
FDMA 30kHz BW
832 Chs FM
1 User/Ch

IS-54/136
TDMA/FDM 30kHz BW
832 Chs $\pi/4$ DQPSK
3 Users/Ch

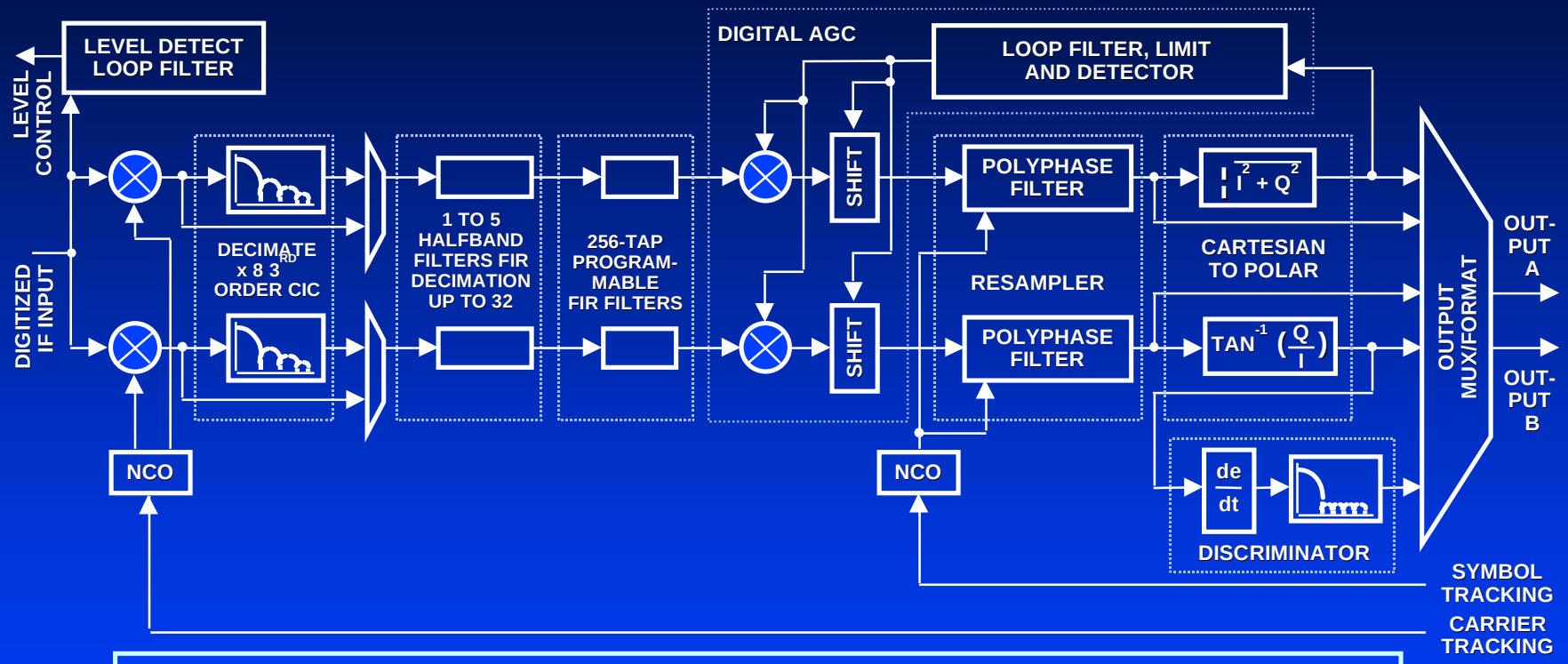
DECT
TDMA/FDM 1.728MHz BW
10 Chs GFSK
12 Users/Ch

DCS 1800
TDMA/FDM 200kHz BW
374 Chs GMSK
8 Users/Ch

What Hardware Works with ALL of These Standards ?

CELLULAR PROVIDER

HSP50214 - Digital IF Downconverter



Features

- UP TO 51.2 Msps INPUT TO SUPPORT WIDEBAND CHANNEL SELECTION
- DIGITAL AGC WITH PROGRAMMABLE LIMITS AND SLEW RATE
- OVERALL DECIMATION FACTOR RANGING FROM 1 TO 2048
- SUPPORTS DEMODULATION OF AM, FM, FSK, DPSK