VLSI AND SOFTWARE RADIOS
By John Fakatselis
Harris semi.
CONTRIBUTING ENABLING TECHNOLOGIES TO VLSI RADIOS

- Process Technology
- Package Technology
- IC Simulation Tools
- System Simulation Tools
• AN EXAMPLE OF A VLSI RADIO DESIGN:

• WIRELESS LAN, BASED ON PROPOSED IEEE8021.11 SPEC.
• RF, IF, MODEM DESIGN, AND PROTOCOL MAC.
Wireless LAN (WLAN) Markets

Current Market
PRIMARILY AT 902 - 928MHz
- MIX OF SPREAD SPECTRUM TRANSCEIVERS WITHOUT STANDARDS
- NO COMPLIANT PROTOCOL STANDARDS
- NO INTEROPERABILITY OF EQUIPMENT
- LOW DATA RATES

Emerging Market
2.4 - 2.5GHz
- IEEE 802.11 STANDARD FOR WLANS
- COMPLIANT STANDARDS FOR INTEROPERABILITY
- CONNECTIVITY
- SUPPORT HIGHER DATA RATES
- PCMCIA LAN CARD SOLUTION
- LOWER COST
- HIGHER PERFORMANCE
  SPEED, RANGE, BATTERY LIFE
The 802.11 Wireless LAN Standard
IEEE 802.11 WLAN Standard

- IEEE WLAN WORKING GROUP WITH GLOBAL REPRESENTATION
- STANDARD FOR WLANS WITH A COMMON MULTI-USER MEDIA
- GLOBAL EQUIPMENT INTEROPERABILITY
- FREQUENCY: 2.4GHz ISM BAND (83.5MHz BW)
- MEDIUM TO HIGH DATA RATES
- APPLICATIONS RANGING FROM SMALL OFFICES TO INDUSTRIAL MANUFACTURING CAMPUSES
- SPREAD SPECTRUM TECHNOLOGY
  - Limits Transmitted Power Density
  - Provides a Robust Solution in a Multi-user Environment
Industrial, Scientific and Medical (ISM) Bands

- UNLICENSED OPERATION GOVERNED BY FCC DOCUMENT 15.247, PART 15
- SPREAD SPECTRUM ALLOWED TO MINIMIZE INTERFERENCE
- 2.4GHz ISM BAND
  - More Bandwidth to Support Higher Data Rates and Number of Channels
  - Available Worldwide
  - Good Balance of Equipment Performance and Cost Compared with 5.725GHz Band
  - IEEE 802.11 Global WLAN Standard
Direct Sequence Spread Spectrum

- DATA SIGNAL SPREAD BY A PN CODE
- PROPERTIES OF PN CODE
- CHIP RATE
- DS PROCESSING GAIN
  \[ G_p (dB) = 10 \log \left( \frac{\text{CHIP RATE}}{\text{DATA RATE}} \right) \]
- PN CORRELATION AT RECEIVER
- PSK DATA MODULATION

![Diagram showing chip rate and correlation]

![Graph showing CW signal and spread signal amplitudes vs frequency]
FSK DATA MODULATION
PERIODIC CHANGES IN THE CARRIER FREQUENCY SPREADS THE SIGNAL
CARRIER FREQUENCY CHANGES AT A SPECIFIED HOP RATE
CARRIER FREQUENCY HOPS AFTER A PRESCRIBED TIME
TOTAL SYSTEM BANDWIDTH INCLUDES ALL OF THE CHANNEL FREQUENCIES USED IN HOPPING
802.11 Protocol Layers

- **Media Access Control Layer**
  - Protocol and Physical Layer Management

- **MAC-PHY Sublayers**
  - Configure data frames and preambles for transmit and receive mode

- **Physical Layer**
  - Radio transmission media for either DSSS, FHSS or infrared
<table>
<thead>
<tr>
<th>Feature</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULATION</td>
<td>DPSK</td>
</tr>
<tr>
<td>PN CODE</td>
<td>11-BIT BARKER</td>
</tr>
<tr>
<td>DATA RATE</td>
<td>1Mbps/DBPSK, 2Mbps/DQPSK</td>
</tr>
<tr>
<td>CHIPPING RATE</td>
<td>11Mcps</td>
</tr>
<tr>
<td>TRANSMIT POWER</td>
<td>USA: 1W MAX.</td>
</tr>
<tr>
<td></td>
<td>EUROPE: 100mW (EIRP)</td>
</tr>
<tr>
<td></td>
<td>JAPAN: 10mW / MHz</td>
</tr>
<tr>
<td>TRANSMIT FREQUENCY TOLERANCE</td>
<td>±25ppm MAX.</td>
</tr>
<tr>
<td>CHIP CLOCK ACCURACY</td>
<td>±25ppm MAX.</td>
</tr>
<tr>
<td>RECEIVER INPUT LEVEL SENSE</td>
<td>-80dBm 8x10^{-2} FER (FRAME ERROR RATE)</td>
</tr>
<tr>
<td>RECEIVER ENERGY DETECT</td>
<td>20µs MAX.</td>
</tr>
<tr>
<td>PREAMBLE LENGTH</td>
<td>144 SYMBOLS</td>
</tr>
<tr>
<td>DATA PACKET SIZE</td>
<td>2048 BYTES MAX.</td>
</tr>
<tr>
<td>ENVIRONMENT</td>
<td>PACKET BURST DATA</td>
</tr>
</tbody>
</table>
WLAN Radio Requirements

- LOW COST
- HIGH DATA RATE AND HIGH THROUGHPUT
- PCMCIA COMPATIBLE
- LONG RANGE
- MOBILITY WITH ROAMING CAPABILITY
- LOW VOLTAGE, LOW POWER, BATTERY OPERATED
- HIGH LEVEL OF INTEGRATION
PRISM™ “Antenna to Bits™”

A Complete DS Spread Spectrum Radio Chipset
RF IC Partitioning Criteria

- FREQUENCY
- ANALOG / DIGITAL SIGNALS
- PROCESS TECHNOLOGY
- ISOLATION REQUIREMENTS
- POWER LEVELS
- PACKAGING
- EXTERNAL COMPONENTS
RF to IF Conversion Issues

- NOISE FIGURE (NF)
- INPUT/OUTPUT 1dB COMPRESSION POINT (IP1dB/OP1dB)
- INPUT/OUTPUT THIRD ORDER INTERCEPT POINT (IP3_i/ IP3_o)
- IMPEDANCE MATCHING
- DYNAMIC RANGE
- SPURIOUS FREE DYNAMIC RANGE (SFDR)
HFA3624 RF to IF Converter

- INTEGRATED RECEIVE / TRANSMIT FRONT END
- 2.4 TO 2.5GHz RF FREQUENCY RANGE
- 10 TO 400MHz IF OPERATION
- SINGLE SUPPLY 2.7V TO 5.5V
- ALL RF I/Os MATCHED TO 50Ω
- INDEPENDENT RECEIVE / TRANSMIT POWER ENABLE

Receive
- LNA
- SINGLE CONVERSION HETERODYNE MIXER

Transmit
- SINGLE CONVERSION MIXER
- LINEAR POWER PREAMP

28-PIN SSOP
- 150mil WIDE
- 0.08 SQUARE INCHES

<table>
<thead>
<tr>
<th>Rx</th>
<th>Tx</th>
<th>POWER CONSUMPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0.3µA</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>48mA</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>18mA</td>
</tr>
</tbody>
</table>

BIAS

AP95358 4-8
HFA3624 Receive Section

LNA @ 2.5GHz
- POWER GAIN ........ 15.6dB
- OP1dB ............... 5.5dBm
- NF .................. 3.8dB

Mixer (LO = 2.15GHz)
- POWER CONVERSION
  GAIN .................. 3.0dB
- IP3 .................. 4.0dB
- NF .................. 12.0dB

NF = 10LOG(F) = NOISE FIGURE
WHERE (F) = NOISE FACTOR
F = SNR_I / SNR_O
HFA3624 RF Front End
Cascaded Performance

Cascaded Performance Data

\[
F_C = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \ldots
\]

- \( F_C \) = CASCADED NOISE FACTOR
- \( G_n \) = GAIN OF STAGE \( n \)

System Performance

- DYNAMIC RANGE (IP1dB - MDS)
- SPURIOUS FREE DYNAMIC RANGE 2/3(IP3_1 - MDS)
- DYNAMIC RANGE (IP1dB - MDS)
- SPURIOUS FREE DYNAMIC RANGE 2/3(IP3_1 - MDS)

\[
\text{MDS} = F_C(kTB)(\text{SNR})_O
\]

where:
- MDS = Minimum Discernible Signal
- \( k \) = Boltzmann’s Constant
- \( T \) = Absolute Temperature in Kelvin
- \( B \) = Bandwidth
- \( (\text{SNR})_O \) = Output Signal-to-Noise Ratio

Cascaded Performance Data

- NF: 4.5dB
- IP1dB: -28dB
- IP3_1: -18dB
HFA3624 Receive Amplifier
Power Gain (S21)

<table>
<thead>
<tr>
<th>FREQUENCY (GHz)</th>
<th>TESTED</th>
<th>SIMULATED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-10</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>-5</td>
<td>-5</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>-5</td>
</tr>
</tbody>
</table>
HFA3624 Transmit Section

**Mixer (Upconverter)**
- POWER CONVERSION GAIN ........ 5.8dB
- LO LEAKAGE ...................... -20.0dB

**Pre-Amp**
- POWER GAIN ..................... 13.0dB
- OP1dB ............................ +7.5dBm

**Cascaded Performance**
- POWER GAIN ..................... 17.8dB
- OP1dB ............................ 0.5dBm
- LO LEAKAGE ..................... -5.0dBm
IF to Baseband Conversion Issues

- PRIMARY SOURCE OF GAIN
  - Limiter or AGC
- RSSI TO MEASURE INPUT SIGNAL
- COMPLEX DOWN CONVERSION TO BASEBAND
- QUADRATURE LO GENERATION
- FILTERING (BASEBAND)
  - Anti-aliasing on Receive
  - Pulse Shaping on Transmit
- UP CONVERSION / MODULATION
- POWER SAVING FEATURES
HFA3724 Quadrature IF Modulator / Demodulator

(A) Limiter and RSSI
- IF UP TO 400MHz
- 84dB GAIN
- 70dB RSSI DYNAMIC RANGE

(B) Demodulator
- DOWN CONVERTS 10 TO 400MHz IF TO BASEBAND
- IN PHASE (I) AND QUADRATURE (Q)

(C) Filter
- TWO LOW PASS FILTERS (I AND Q)
- DIGITALLY SELECTABLE FILTER CUTOFF
- MULTIPLEXED RECEIVE / TRANSMIT

(D) Modulator
- UP CONVERT AND PHASE MODULATES I AND Q TO 300MHz

(E) Power
- POWER CONTROL INCORPORATING SLEEP MODE
- HALF DUPLEX OPERATION

AP96358 4-16
**HFA3724 Limiter and RSSI**

**Limiter**
- TWO INDEPENDENT AMPLIFIERS
- GAIN (EACH AMP) FROM 10 TO 400MHz .......... 42dB
- LIMITER -3dB SENSITIVITY ................. -84dBm
- NF (FOR 250Ω SINGLE ENDED INPUT IMPEDANCE) ............. 6dB

**RSSI**
- SENSITIVITY ................. -84dBm
- DYNAMIC RANGE ............ 70dB
- RSSI SLOPE ................. 5μA/dB
HFA3724 Q-Modem

Quadrature Downconverter
- INPUT FREQUENCY RESPONSE: 400MHz
- DIFFERENTIAL VOLTAGE GAIN: 8dB
- PHASE MATCH: ±2°
- AMPLITUDE MATCH: ±0.5dB

Quadrature LO Generator
- INTERNAL DIVIDE BY 2 FLIP-FLOP WITH DUTY CYCLE COMPENSATION
- 50Ω DIVIDED BUFFER OUTPUT AVAILABLE

Quadrature Upconverter
- PHASE MATCH: ±2°
- AMPLITUDE MATCH: ±0.5dB
- LO LEAKAGE: -30dBc
- MINIMUM SIDEBAND SUPPRESSION: (400MHz) 26dBc
HFA3724 Baseband Filters

- 5 - POLE BUTTERWORTH FILTERS
- MULTIPLEXED FILTERS FOR HALF DUPLEX OPERATION
  - Pulse Shaping on Transmit
  - Anti-aliasing on Receive
- FOUR SELECTABLE CUTOFF
- FREQUENCIES: 2.2MHz, 4.4MHz, 8.8MHz, 17.6MHz
- ± 20% FINE TUNING WITH EXTERNAL RESISTOR

- TRANSMIT FILTERING REDUCES SPECTRAL PRODUCTS TO IEEE802.11 SPECIFIED LEVELS
- TUNING RESISTOR COMPENSATES FOR SPECTRAL RE-GROWTH
Adjacent Channel Interference Versus Intersymbol Interference

RF FREQUENCY SPECTRUM

CHANNEL BANDWIDTH

NARROWBAND FILTER

WIDEBAND FILTER

EYE DIAGRAM OF DATA
THEORETICAL AMPLITUDE AND GROUP DELAY OF FOUR DIFFERENT FILTERS
FILTERS ARE 5 POLE
CUTOFF FREQUENCY NORMALIZED TO 1kHz
Filter Cutoff Frequency Selection

ATTENUATION (dB)

FREQUENCY (MHz)

<table>
<thead>
<tr>
<th>SEL 1</th>
<th>SEL 0</th>
<th>f_{3dB} (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>2.2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>4.4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>8.8</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>17.6</td>
</tr>
</tbody>
</table>
HFA3724 Performance Data

Modulator Output

POWER (dBm)

-24
-44
-64
-84

FREQUENCY (MHz)

255 280 305

-28dBm

Modulator Output with Filter Tuning Resistor

POWER (dBm)

-24
-44
-64
-84

FREQUENCY (MHz)

255 280 305

-36dBm

AP96358 4-23
Baseband Section Issues

- ANALOG TO DIGITAL CONVERSION
- SPREAD / DESPREAD
- MODULATE / DEMODULATE
- CLEAR CHANNEL ASSESSMENT
- DATA FORMATTING AND HEADER CREATION

HSP3824
BASEBAND PROCESSOR

DUAL SYNTHESIZER

ADC
I ADC
Q ADC
SPREAD
MODULATE/ ENCODE
DE- SPREAD
DE- MODULATE
Tx/Rx DATA I/O
CONTROL - TEST I/O
HSP3824 Analog to Digital Converters

- 44Msps, 3-BIT FLASH A/Ds SAMPLE I/Q INPUTS
- PATENTED CIRCUITRY ACTS AS AGC TO KEEP A/Ds AT FULL SCALE

- 2Msps, 6-BIT A/D SAMPLES RSSI
Why 3-Bits?

- 3-BIT QUANTIZATION GIVES SIGNIFICANT ADVANTAGE OVER 1-BIT
- QUANTIZATION TO GREATER THAN 3-BITS YIELDS NEGLIGIBLE IMPROVEMENT

Correlator SNR₀ vs SNRᵢ

- Expected operating point of 10⁻⁵ BER
- Quantization Q = 8 (3-BIT)
- Quantization Q = 2
- SNR₀ (3dB/DIV)
- SNRᵢ (3dB/DIV)
HSP3824 Matched Filter Correlator

Rx DATA FROM ADCs

2x CHIP CLOCK

PARALLEL PN REGISTER LOAD

Z₁⁻¹ → Z₂⁻¹ → Z₃⁻¹ → Z₄⁻¹ → Z₅⁻¹ → Z₆⁻¹ → Z₂ᴺ⁻¹

R₁ → R₂ → R₃ → Rᴺ

N = 16

Σ

11-BIT BARKER CODE EXAMPLE:
+1 -1 +1 +1 -1 +1 +1 +1 -1 -1 -1 +1 -1 +1 +1 -1 +1 +1 +1 -1 -1 -1

A/D SAMPLE CLOCK

CHIP PERIOD

SYMBOL PERIOD

CORRELATION SCORE

AP96358 4:33
DPSK Demodulator

- COHERENT LOOP FOR PHASE ERROR COMPENSATION
- USER CONFIGURABLE SIGNAL QUALITY THRESHOLDS
Complete RF to Baseband Circuit

- **LNA Used to Increase Gain 8 to 10dB**
- **Two Pole Dielectric or LC Filter**
  - $f_0 = 2.4\,\text{GHz}$
  - $\text{BW} = 80\,\text{MHz}$
- **VCO Oscillator Set for 2.21 to 2.22GHz LO**
- **VCO Oscillator Set for 560MHz**
- **Transmit Section**
  - **HFA3925 RF Power Amplifier and Tx/Rx Switch**
  - **HFA3624 RF/IF**
  - **HFA3524 Dual Synthesizer**
  - **Synthesizer Control from MAC**
- **Receive Section**
  - **HFA3724 Quadrature Demodulator**
  - **Filter Cutoff Selection**
  - **Limit 1/Limiter 2 Interstage BPF**
  - $f_0 = 280\,\text{MHz}$
  - $\text{BW} = 17\,\text{MHz}$
- **SAW Filter**
  - $f_0 = 280\,\text{MHz}$
  - $\text{BW} = 17\,\text{MHz}$
- **Two Pole Dielectric or LC Filter**
  - $f_0 = 2.4\,\text{GHz}$
  - $\text{BW} = 80\,\text{MHz}$
- **VCO Oscillator Set for 2.21 to 2.22GHz LO**
MAC-PHY Glueless Interface

HSP3824

Tx_PE
TxD
TxCLK
Tx_RDY
CCA
RxD
RxC
MD_RDY

Serial Control Bus
CS
SD
SCLK
R/W
AS

ANTSEL

Synthesizer Control
TO HFA3524

TxCMD
TxDATA
TxC
INT1
INT2
RxDATA
RxCIN
MD_RDY
I/O Control Port

TO HFA3624/3724

TxPE
RxPE

TO HFA3724

Filter Cutoff Selection

AM79C930VC
AMD
PC-NET
Mobile MAC

Tx/Rx Power Control

RAM

ROM

PC Interface

RAM

ROM

TO HFA3624/3724

Sele 0

Sele 1

ANTSEL

Synthesizer Control

CLOCK
DATA
STB

Sel 0

Sel 1

TO HFA3724

Filter Cutoff Selection

Sele 0

Sele 1

TO HFA3624/3724

TxPE
RxPE

PC Interface

RAM

ROM
HSP3824 Evaluation Setup

- **HP8780A VECTOR SIGNAL GENERATOR**
  - 280MHz
  - BASEBAND DATA
  - CARRIER
  - CLOCK GENERATOR
  - IBM-PC CONTROL
  - TQ
  - TxQ

- **NOISE/COM 6108 (NOISE ADDER)**
  - 280MHz
  - S + N
  - PAD

- **HP8981 VECTOR SIGNAL ANALYZER**
  - 280MHz
  - I OUT
  - Q OUT
  - CARRIER
  - BASEBAND DATA
  - HP8657B SIGNAL GENERATOR

- **FIREBERD 6000A BER TESTER**
  - BERT
  - CONTROL PORT
  - FIREBERD 6000A EVALUATION BOARD
  - TQ

- **IBM-PC CONTROL**

- **CONTROL PORT**
  - HSP3824 EVALUATION BOARD
  - TQ

- **CONTROL PORT**
  - HSP3824 EVALUATION BOARD
  - RxQ

- **BASEBAND DATA**

- **VECTOR SIGNAL GENERATOR**

- **NOISE/COM 6108 (NOISE ADDER)**

- **HP8981 VECTOR SIGNAL ANALYZER**

- **FIREBERD 6000A BER TESTER**

- **IBM-PC CONTROL**

- **CONTROL PORT**
  - HSP3824 EVALUATION BOARD
  - RxQ
## BER Performance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>LOSS IN dB @ 10^{-5} BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHASE NOISE</td>
<td>*</td>
</tr>
<tr>
<td>LIMITING AMPLIFIERS IN IF</td>
<td>0.5</td>
</tr>
<tr>
<td>I/Q PHASE AND AMPLITUDE IMBALANCE</td>
<td>0.75</td>
</tr>
<tr>
<td>A/D LINEARITY</td>
<td>NEGLIGIBLE</td>
</tr>
<tr>
<td>A/D HEADROOM vs BIAS ADJUSTMENT</td>
<td>NEGLIGIBLE</td>
</tr>
<tr>
<td>OSCILLATOR OFFSET IN CORRELATOR AT 50ppm</td>
<td>0.22</td>
</tr>
<tr>
<td>SAMPLING STRADDLING OFFSET AND IF + LPF FILTER LOSSES</td>
<td>2.0</td>
</tr>
<tr>
<td>QUANTIZATION AND DQPSK DEMOD LOSS</td>
<td>0.5</td>
</tr>
<tr>
<td>PHASE LOCK LOOP NOISE</td>
<td>0.1</td>
</tr>
<tr>
<td>DESCRAMBLER ERROR EXTENSION</td>
<td>0.5</td>
</tr>
</tbody>
</table>

* Depends on synthesiser

**BER vs E_b/N_o Performance**

![Graph](image)

- **DBPSK**
- **DQPSK**
- **THEORY (DBPSK)**

*Depends on synthesiser*
HSP3824 Transmit Section

DPSK Modulator

- FOUR SELECTABLE, INTERNALLY GENERATED PREAMBLE/HEADER FORMATS
- SELECTABLE CHIP SEQUENCES OF 11, 13, 15 OR 16 CHIPS PER SYMBOL
- SYMBOL RATE = MCLK/(N * CHIPS PER SYMBOL)
  WHERE MCLK = SAMPLE RATE CLOCK AND N IS A PROGRAMMABLE DIVIDER OF 2, 4, 8 OR 16
RF Power Amplifier Issues

- POWER GAIN
- POWER ADDED EFFICIENCY
- 1dB COMPRESSION
- IMPEDANCE MATCHING
- SUPPLY VOLTAGE

HFA3925
RF POWER AMPLIFIER AND Tx/Rx SWITCH

DUAL SYNTHESIZER
HFA3925 RF Power Amplifier and Switch

- HIGHLY INTEGRATED GaAs POWER AMPLIFIER WITH T/R SWITCH
- HIGH LINEAR OUTPUT POWER AT OP1dB 24dBm (250mW)
- INDIVIDUAL GATE CONTROL FOR EACH AMPLIFIER STAGE
- VSWR IN/OUT . . . . . . . 1.75:1
- SUPPLY VOLTAGE ... 2.7 TO 6V
- T/R SWITCH
  - Insertion Loss . . . . . . . 1.2dB
  - Isolation . . . . . . . . . . . . 12dB

28 Lead SSOP
Complete Baseband to RF Circuit

- **HFA3925**: RF Power Amplifier and Tx/Rx Switch
- **HFA3624**: RF/IF Section
- **HFA3524**: Dual Synthesizer
  - VCO Set to 2.21 to 2.22GHz LO
  - VCO Set for 560MHz LO
- **HFA3724**: Quadrature Modulator
  - Digital I/Q Data Received from BBP
  - 5th Order Butterworth Low-Pass Filter
- **IF BP Filter**: $f_0 = 280$MHz, BW = 17MHz
- **TWO POLE DIELECTRIC FILTER**: $f_0 = 2.4$GHz, BW = 80MHz
- **THREE POLE DIELECTRIC FILTER**: $f_0 = 2.4$GHz, BW = 80MHz
- **RECEIVE SECTION**: 5th Order Butterworth Low-Pass Filter
- **DIGITAL I/Q DATA RECEIVED FROM BBP**: Receive Section

---

AP96358 4-44
SOFTWARE RADIOS

- PROGRAMMABLE RADIOS TO ACCOMODATE VARIOUS MODULATION REQUIREMENTS.
- DIGITAL SIGNAL PROCESSING TECHNIQUES.
- DIGITAL FILTERING TECHNIQUES.
Summary of Cellular and PCS Standards

**IS-95**
- CDMA/FDM 1.25MHz BW
- 20 Chs
- BPSK/OQPSK
- 798 Users/Ch

**GSM**
- TDMA/FDM 200kHz BW
- 124 Chs
- GMSK
- 8 Users/Ch

**AMPS**
- FDMA 30kHz BW
- 832 Chs
- FM
- 1 User/Ch

**DECT**
- TDMA/FDM 1.728MHz BW
- 10 Chs
- GFSK
- 12 Users/Ch

**IS-54/136**
- TDMA/FDM 30kHz BW
- 832 Chs
- \(\pi/4\) DQPSK
- 3 Users/Ch

**DCS 1800**
- TDMA/FDM 200kHz BW
- 374 Chs
- GMSK
- 8 Users/Ch

What Hardware Works with ALL of These Standards?
HSP50214 - Digital IF Downconverter

Features
- UP TO 51.2 Msps INPUT TO SUPPORT WIDEBAND CHANNEL SELECTION
- DIGITAL AGC WITH PROGRAMMABLE LIMITS AND SLEW RATE
- OVERALL DECIMATION FACTOR RANGING FROM 1 TO 2048
- SUPPORTS DEMODULATION OF AM, FM, FSK, DPSK