DSP IMPLEMENTATION OF HIGH SPEED WLAN USING OFDM

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OFDM has been chosen in all three of the world’s 5 GHz wireless LAN standards (Hiperlan/2, IEEE 802.11a and HiSWANa). Each standard operates using adaptive QAM sub-band modulation and offers a peak data rate of 54 Mbits/s using 20 MHz of bandwidth.

This presentation describes a real-time DSP implementation of an asynchronous OFDM QPSK based physical layer platform using the Texas Instruments fixed-point DSP TMS320C620. The performance of the system has been evaluated in AWGN and ETSI BRAN indoor channel ‘A’ with 50ns of RMS delay spread. The results shown an uncoded Bit Error Rate (BER) of 1 in 1000 at 10 dB Signal to Noise Ratio (SNR) per symbol in AWGN. In ETSI Channel ‘A’, an uncoded error floor occurs at a BER of 2 in 1000 at 30 dB SNR per symbol.

A 10-bit Analogue to Digital Converter (ADC) has been used in the receiver. The limited number of bits in the ADC in the presence of sampling noise reduces the dynamic range of the receiver. In Rayleigh fading channels, this leads to the erroneous calculation of the Channel State Information vector and hence the creation of an uncoded error floor. This error floor can be reduced by increasing the number of bits in the ADC or by the application of FEC (as specified in the standards).
## Summary of Main Modem Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Channel bandwidth</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Modulation scheme</td>
<td>OFDM QPSK</td>
</tr>
<tr>
<td>Data payload rate</td>
<td>24 Mbits/s</td>
</tr>
<tr>
<td>Number of subcarriers</td>
<td>48</td>
</tr>
<tr>
<td>Number of pilot subcarriers</td>
<td>4</td>
</tr>
<tr>
<td>Subcarrier frequency spacing</td>
<td>0.3125 MHz</td>
</tr>
<tr>
<td>IFFT/FFT points</td>
<td>64</td>
</tr>
<tr>
<td>IFFT/FFT period</td>
<td>3.2 us</td>
</tr>
<tr>
<td>Preamble duration</td>
<td>8 us</td>
</tr>
<tr>
<td>Guard interval</td>
<td>0.8 us</td>
</tr>
<tr>
<td>Symbol interval</td>
<td>4 us</td>
</tr>
<tr>
<td>Symbols per packet</td>
<td>23</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Coding scheme</td>
<td>None</td>
</tr>
</tbody>
</table>
Block Diagram of the System

- Binary data
- Scramble binary data
- IFFT preamble
- Insert cyclic prefix
- Modulate control symbol
- IFFT control symbol
- Insert cyclic prefix
- Modulate data symbols
- IFFT data symbols
- Insert cyclic prefix
- Wideband channel
- AWGN
- FFT preamble
- FFT control symbol
- Equalise control symbol
- Equalise data symbols
- Calculate channel state information
- Demod control symbol
- Demod data symbols
- Descramble binary data
- Binary data
- Sync + Packet Number
- Data (20 OFDM symbols)
- Preamble
- Preamble
- From Transmitter PC
- To Receiver PC
- 92 µs

ETSI BRAN Channel A (50 ns RMS, NLOS)
Hardware Prototype

Bits per packet = 20 x 48 x 2 = 1920
Packets per frame = 160
Bits per frame = 307200
Delay per frame:
DMA initialisation delay = 15 μs
Sampling delay = 135 μs
Mod/Demod delay = 500μs x 160
Data transfer delay = 10 ms
Samples store delay = 10 μs
Total delay = 181.6 ms

Turn around time (for TDD) = 181.6ms /160 x 2 = 2.27 ms
Duty cycle = 1.7 / 24 = 7 %
Sustained data rate = 1.7 Mbit/s
Daughter Board Layout

Legend:
AAF (I/Q): Anti Aliasing Filter
LPF (I/Q): Low Pass Filter (for reconstruction)
ADC: Analogue to Digital Converter
DAC: Digital to Analogue Converter
GUI of the TxPC software and RxPC software

Communication mode:
- Video Transmission
- PN Sequence Transmission (to calculate BER)

Connection modes:
- No Channel
- AWGN
- ETSI BRAN Channel A (50 ns RMS, NLOS)
Results: Performance in AWGN channel

Difference = less than 0.5 dB
Results: Performance in ETSI BRAN Channel A

Error Floor at 30 dB

Difference = 2.5 dB
Consequences of Error Floor

- Impossible to recover data in deep sub-band fades
- Uncoded system without error floor difficult to achieve
- Higher level modulation schemes face more severe error floors

Recommendations to lower/remove Error Floor

- Increase number of bits in ADC
- Employ FEC to correct sub-band errors
Conclusions

- A real-time implementation of an OFDM based Wireless LAN system has been generated using the TMS320C62.
- A custom daughter board has been designed to offer buffer memory and high speed A/D and D/A conversion.
- In AWGN, the modem performs to within 0.5 dB of the floating point simulation result.
- A peak data rate of 24 Mb/s is achieved on a burst by burst basis assuming a 20 MHz bandwidth and a 64 carrier QPSK modem.
- A sustained uncoded user data rate of 1.7 Mb/s (7% duty cycle) is achieved.
Conclusions

- In IEEE/ETSI channel ‘A’ (50ns RMS delay spread), an error floor occurs due to insufficient digital dynamic range in the receiver.

- This error floor can be removed by FEC coding, however the floor will become more severe for higher level modulation.

- Uncompressed (1.5 Mb/s) and compressed (H263+ at 100 kb/s) video streams have been sent over the demonstration system.

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Future Work

- Real Time RF Transmission
- Exploitation of Antenna Arrays
- Integrated Error Resilient Video
- Space-Time Coding
- Channel Characterisation
- MIMO OFDM (>500 Mb/s WLANs)
- Exploitation of Antenna Arrays
- Space-Time Coding
- MIMO OFDM (>500 Mb/s WLANs)

Circular Rx array

Medav sounder

Circular Tx array